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MODULAR MULTI-SENSOR DISPLAY SYSTEM DESIGN STUDY

Volume II Detail Design and Application Analysis

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AIR FORCE SYSTEMS COMMAND
WRIGHT—PATTERSON AIR FORCE BASE, OHIO 45433

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A study of the requirements for and the design of a Modular Multi Sensor Display System was conducted. The purpose of the study was to perform the functional design of core and special module, that, when integrated together, perform the digital scan conversion, digital symbol generation, and display functions of multiple Air Force Avionics Systems. Specifically, the requirements were derived from the avionics sensor systems aboard F-4, A-7, F-106, F-111 and B-1 type aircraft. An analysis

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Item 20. Abstract (continued)

was also performed to insure that the design was compatible with the spatial resolution, dynamic range and temporal response of the human operator.

The design study resulted in the definition of 20 core modules with universal system applicability and six special modules to perform specific interface and special mode functions. The resulting design was partitioned onto both LSI modules and discrete MSI printed circuit card modules. A programmable controller was designed to allow simple modification and growth for both the scan converter and symbol generator.

A tradeoff analysis was conducted to compare the modular design with existing analog techniques and with a discrete digital design to meet the specific display system requirements of the A-7 aircraft. Physical characteristics, cost of ownership, reliability, and maintainability were the key factors of this tradeoff. The modular design, although consisting of more circuitry to provide the multi-system flexibility, provides significantly improved reliability over the analog design and has a lower cost of ownership than the other alternatives. The lower cost is due to reduced development costs since "off the shelf" modules can be used, and to lower module costs due to the larger quantities produced. The recommendation from this study is the development of a MMSDS brassboard to demonstrate the modular concept and to evaluate the programmable controller functions as applied to various avionics systems.

FOREWORD

This report, submitted May 1974, covers the work accomplished during the period of May 21, 1973 through February 21, 1974 under Contract F33615-63-C-1267, 20030606, Modular Multi-Sensor Display System Design Study. The work was supported by the United States Air Force Avionics Laboratory (AFAL), Wright Patterson Air Force Base, Dayton, Ohio. The Technical Monitor was Mr. S. H. Young of AFAL/AAM. The report is divided into three volumes: Vol. I Requirements Analysis and Design Studies, Vol. II Detail Design and Applications Analysis, and Vol. III Tabulation of Sensor - Display Parameters. (Confidential)

The work was accomplished by the Display Systems and Human Factors Department of Hughes Aircraft Company under the direction of Mr. J. L. Heard as Program Manager and Mr. E. W. Opittek as Project Engineer. Special acknowledgement is given to the following individuals for their contributions to this report.

Mr. W. C. Hoffman acted as technical consultant and performed a major editing function. Messrs. W. L. Carel, S. J. Vanderkolk and Mr. M. Hershberger were responsible for defining the operator requirements. Mr. G. Wolfson was responsible for the contrast enhancement analysis and symbol generator tradeoffs. Mr. B. W. Keller was responsible for the detail module design with assistance from Messrs. M. D. Pruznick, S. E. Whiteside, J. R. Phelps, and R. M. Smithers. Mr. E. J. Dragavon performed the sensor criteria analysis and the actual research and tabulation of the sensor parameters was achieved by Mr. J. Stoltz. Mr. J. L. Bellock performed the cost of ownership and reliability analysis. Ms Anita Stoudt assisted in the report preparation.

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1.0 INTRODUCTION AND SUMMARY

1.1 Background

The display of data from a variety of sensors having different data rates and formats on a common indicator has always been attractive and has resulted in the development over the past several years of a progression of multi-mode display systems ranging from dual-persistence cathode-ray-tubes to direct view storage tubes, analog scan converter tubes and digital scan conversion techniques. Numerous studies and applications have shown that a scan conversion function along with a high performance television compatible CRT display provides the best potential performance and flexibility. However, experience with analog scan conversion in field applications has demonstrated an inherent low reliability, poor performance and high cost of ownership.

Developments in digital technology, particularly in solid state memories and in MSI/LSI packaging density has made the implementation of a totally digital scan converter a reality. This all digital mechanization provides an inherent improvement in reliability, maintainability, and flexibility with a significantly reduced cost of ownership. Several specific designs of digital scan converter/display systems for particular aircraft systems have already been proposed. The purpose of this study was to expand the specific design concepts to a modular scan converter/display system which would be compatible with multiple aircraft configurations including both current systems and future applications.

Such a modular design would be comprised of certain core modules which would be combined together to meet the requirements of various existing and new aircraft. Also, special modules unique to a specific system or mode would be designed as required. The advantages of such an approach include: lower cost of ownership due to minimized new system development and lower maintenance, spares, and training costs; increased reliability over existing analog systems; adaptability to new digital display and processing techniques.

1.2 Study Program

The modular multi-sensor display system (MMSDS) study program consisted of six major tasks:

1. A sensor display requirements analysis based on a survey and tabulation of the parameters of several existing or projected Air Force avionics sensor systems.

2. An evaluation of the human operator characteristics and their effect on the display design requirements.

3. The development of design criteria for determining the performance of a display system with respect to the sensor and operator characteristics.

4. The evaluation of alternate design mechanizations to determine an optimum design approach.

5. The functional design, partitioning and detail design of the MMSDS core and special modules.

6. An analysis of the application of the MMSDS to a specific avionics system to determine the cost and advantages of the MMSDS design.

The structure of this report follows the task organization.

Volume I is dedicated to requirements analysis and design studies.

Section 2.0 (Volume I), Functional Requirements, documents the results of task 1 and 2 and provides a complete summary of the sensor parameters for 25 radar and electro-optical systems and the human operator characteristics in terms of spatial resolution, dynamic range and temporal response. These parameters form the basis of the MMSDS design requirements and are tabulated in Table 1.

TABLE 1. SUMMARY OF DISPLAY SYSTEM FUNCTIONAL REQUIREMENTS

Display Formats

Radar

Air-to-air B-scan

Ground map sector PPI

Expanded sector PPI

Squinted side looking strip map

High resolution ground map patch

Air-to-ground ranging

Terrain following E-Square scan

Electro-Optical

Down looking line scan strip map

Air-to-air IR C-scan

Forward looking infra-red (FLIR) raster

Television raster

(Continued next page)

(Table 1, continued)

Sensor Parameters

Radar

Range	1.0 - 200 n.mi.
PRF	300 - 5000 hz
Az/El Beamwidth	0.5 to 10°
Az Scan Limits	±90°
El Scan Limits	±60°
Scan Rates (Az & El)	50 to 250 deg/sec
Pulse Width	0.1 to 2.5 μsec
Video BW	0.5 to 10 Mhz
Dynamic Range	20 - 40 db

Electro-Optical (EO)

TV Bandwidth	5 - 25 Mhz
Dynamic Range	40 - 100 db
EO Line Scan Rate	500 - 2000 Hz
Scan Angle	±60°
EO Line Scan BW	Up to 1 Mhz
Number of Line Scan Detectors	1 to 10

Operator Requirements

Radar display

Active Raster Lines	≅100 per inch
Pixels per Inch	>50, <100
Dynamic Range	>10:1, <1000:1
Gray Scale Quantization	≧2 bits (4 shades)
Average Effective Luminance, fL	>0.05 x adaptation luminance (day), ≧0.1 fL (night)
Phosphor Color	Green
Frame Rate	30 Hz

(Continued on next page)

(Table 1, concluded)

Operator Requirements (Continued)

Electro-Optical display

Characteristics	Analog Display	Quantized Display
Active Raster Lines	≅100 per inch	≅100 per inch
Pixels per Inch	N. A.	>50, <100
Dynamic Range	>100:1, <1000:1	>100:1, <1000:1
Gray Scale Quantization	N. A.	≥4 bits (16 shades)
Average Effective Luminance, fL	>0.05 x adaptation luminance (day), ≥0.1 fL (night)	>0.05 x adaptation luminance (day), ≥0.1 fL (night)
Phosphor Color	Green	Green
Frame Rate	30 Hz	30 Hz

Section 3.0 (Volume I), Design Performance Criteria, relates the performance requirements to the mechanization parameters and provides the design tools necessary to evaluate alternate mechanizations and optimize the design approach. Specific mechanization parameters such as A/D converter sampling frequency, memory size and display size are determined from the sensor parameters such as pulse width, range scale and display format.

Section 4.0 (Volume I), Mechanization Tradeoffs, contains the major design trade studies which were performed to determine the optimum design approach. Tradeoffs were made in five major areas: 1) selection of display sweep formats, 2) determination of basic scan converter architecture, 3) selection of memory tape, size and structure, 4) determination of digital scan converter controller architecture, 5) determination of optimum symbol generator configuration. A summary of the major conclusions arrived at as a result of the tradeoff studies is given in Table 2.

Volume II of the report is dedicated to the detail module design and application tradeoff analyses. The detail design and partitioning of the core and special modules based on meeting the requirements are presented in Section 2.0 of Volume II.

Section 3.0 (Volume II), Applications Analysis, shows how the "core" and "special" modules are configured for various avionics systems. A comparison of three display systems configured for the A-7 aircraft is presented which evaluate an analog scan converter/display, a digital scan converter/display and the modular-multisensor display system (MMSDS). Physical parameters, cost, reliability, and maintainability were the major parameters

compared. A cost of ownership analysis, reliability analysis and physical system description are also included in this section.

Volume III is a classified volume (Confidential), listing the pertinent sensor parameters used to derive the MMSDS mechanization parameters.

TABLE 2. CONCLUSIONS FROM DESIGN TRADEOFF STUDIES

- Display all video and symbology in a horizontal television format.
- Utilize a data bus control architecture with separate memory, integrator, and controller.
- Use MOS random access solid state memory.
- Use microprocessor type controller, programmable to provide mode and system modifications.
- Generate symbols in-raster using programmable chain type symbol generator.

1.3 Recommended Design

The results of the system design and application analysis indicates that the modular multi-sensor display concept does provide a lower cost of ownership system. The recommended design is shown in Figure 1. It consists of a digital scan converter and digital symbol generator both of which operate under control of identical microprocessor controllers. Changing of modes, parameters and growth are achieved by reprogramming the memory portion of the controllers without any hardware changes. Increased resolution is obtained by expanding the modular display refresh memory. Input radar video in any format is digitized, processed and buffer stored in the integrator and stored in the digital memory. Besides the radar conversion, line scan EO video can also be scan converted and a frame of TV or FLIR video can be frozen for more detailed viewing. Readout of the memory is achieved in a standard television raster format providing composite video interface and easy recording on video tape. The modular display indicator unit is capable of displaying video in a horizontal television type raster of from 525 to 1023 lines. The display CRT module is selected based on the resolution required and the physical limitation of the cockpit installation. A programmable chain type symbol generator permits the presentation of any symbol shape and symbol repertoire mixed in the TV raster. Input control signals are accepted from either the standard Air Force Digital Avionics Interface System (DAIS) bus MUX interfaces or through special interface modules designed to convert existing system interfaces to a digital parallel format. DAIS is the Air Force advanced concept to provide a mission flexible total information management system consisting of modular subsystems. A summary description of the "core" and "special" modules is provided in the following paragraphs.

1.3.1 Digital Signal Transfer Unit Core Modules

1. Video Receivers and A/D - Buffers and translates input video and syncs to digital TTL logic levels.

2. Integrator and Truncator Memory - Memory module used with input radar video processing functions.

3. Integrator, Peak Detector and Truncation Logic - Processes input radar video to optimize characteristics of digitally sampled video.

4. Controller - Programmable microprocessor type controller to generate all mode, built-in-test, and control signals to both the scan converter and symbol generator functions. Two identical controllers can perform this function. The input control interface to the DAIS is also provided in this module.

5. Controller Memory - Storage for all system control programs. Mode and system parameter modifications can be made by reprogramming this module.

6. Display Refresh Memory - Modular memory for storage of digitized radar or EO video and symbology. Basic module stores 256 x 256 elements and contains all necessary input and output logic.

7. Memory Input Address Generator - High speed logic module commanded by system controller to generate memory load address sequences as a function of format.

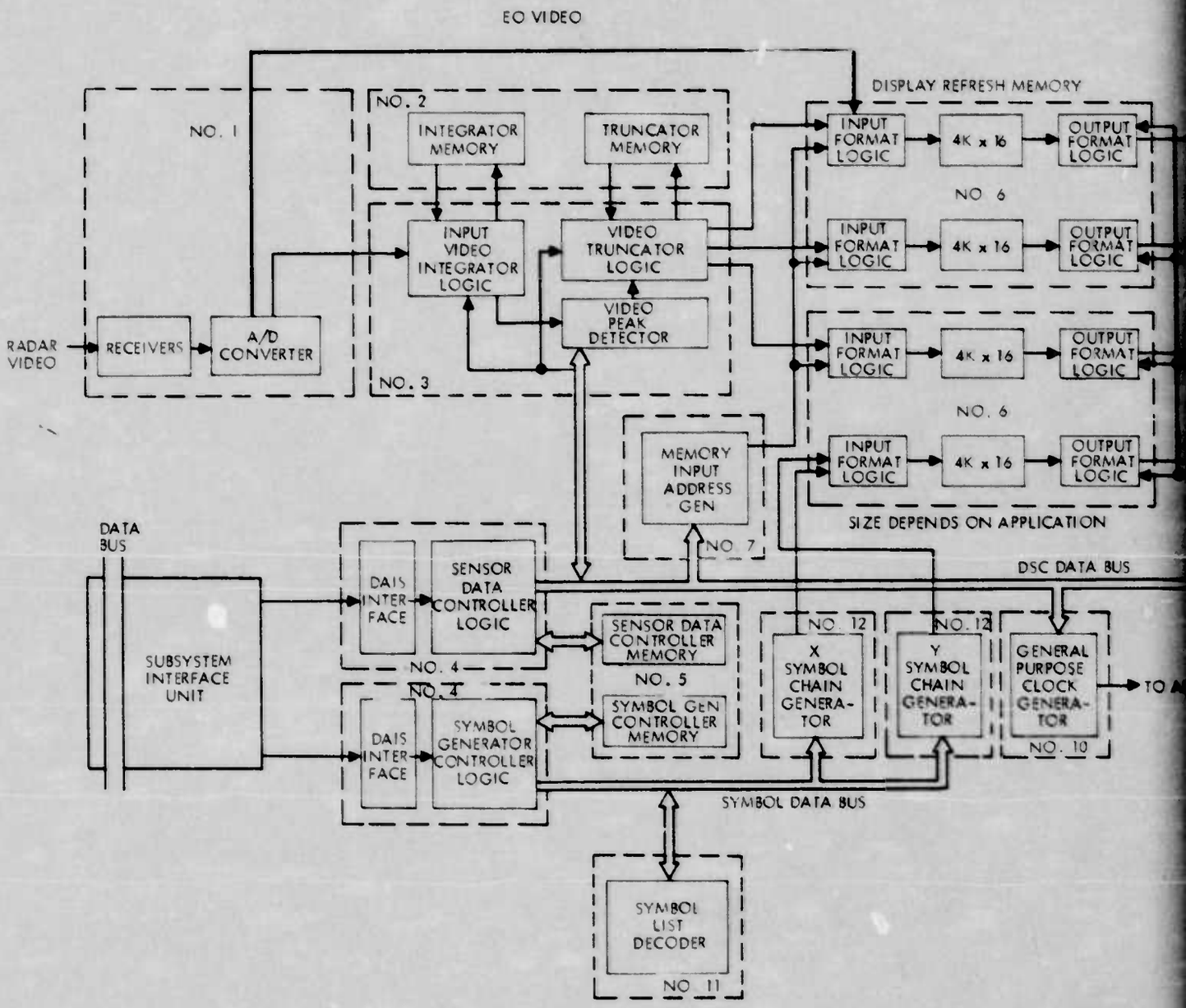
8. Memory Output Address and Display Sync Generator - Generates read address to display refresh memory to provide television raster compatible video. Also generates standard EIA composite syncs.

9. Output Video Processing - Performs output video D/A conversion, sync and symbol mixing, filtering and gamma shaping to optimally match the display CRT transfer function.

10. Clock Generator - Generates all necessary system clock rates and phases under command of the system controller.

11. Symbol List Decoder - Transforms symbol control signals to command signals to the symbol chain generators.

12. Symbol Chain Generator - Two identical X and Y modules generate X and Y addresses to the symbol refresh portion of the Display Refresh memory.


EO VIDEO
DISPLAY REFRESH MEMORY
NO. 1
NO. 2
INTEGRATOR MEMORY
TRUNCATOR MEMORY
INPUT VIDEO INTEGRATOR LOGIC
VIDEO TRUNCATOR LOGIC
VIDEO PEAK DETECTOR
NO. 3
RADAR VIDEO
RECEIVERS
A/D CONVERTER
INPUT FORMAT LOGIC
4K x 16
OUTPUT FORMAT LOGIC
NO. 6
NO. 6
SIZE DEPENDS ON APPLICATION
MEMORY INPUT ADDRESS GEN
NO. 7
DATA BUS
SUBSYSTEM INTERFACE UNIT
DAIS INTER-FACE
SENSOR DATA CONTROLLER LOGIC
NO. 4
SENSOR DATA CONTROLLER MEMORY
NO. 5
SYMBOL GEN CONTROLLER MEMORY
NO. 4
DAIS INTER-FACE
SYMBOL GENERATOR CONTROLLER LOGIC
DSC DATA BUS
NO. 12
X SYMBOL CHAIN GENERA-TOR
NO. 12
Y SYMBOL CHAIN GENERA-TOR
GENERAL PURPOSE CLOCK GENERA-TOR
NO. 10
TO A
SYMBOL DATA BUS
SYMBOL LIST DECODER
NO. 11

2

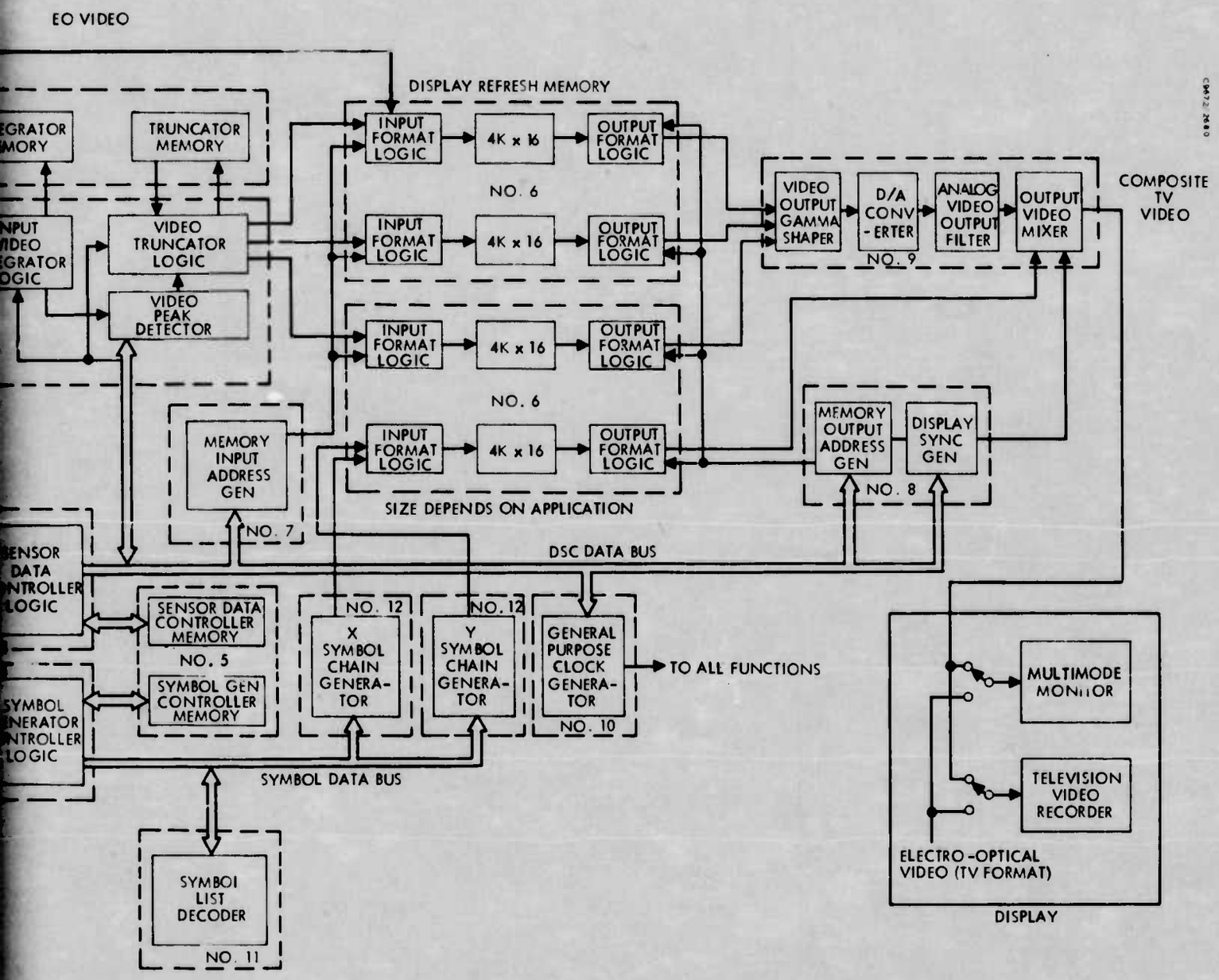


Figure 1. Partitioned modular display system.

1.3.2 Digital Signal Transfer Unit Special Modules

1. Non DAIS Interface Module - Converts analog signals, synchro signals, etc., to the digital parallel format required by the MMSDS system controllers.

2. Special Purpose Clock Generator - Generates variable clock rates to perform such special functions as ground range sweep correction and terrain following E^2 displays.

3. Video Processing Module - A histogram equalization module is described which enhances the radar video display. Other video processing modules may also be designed.

4. Out of Scan Blanking Module - Generates display blanking signal for area outside the limits of the PPI radar scan pattern.

5. Video Aging Module - Allows generation of variable persistence type of display presentation on multiple frame processed air-to-air search display.

1.3.3 Multi Mode Display Core Modules

1. Video Amplifier/Blanking Module - Receives selected composite video, strips off syncs and drives the CRT control grid.

2. Horizontal AFC/Deflection Module - Generates horizontal sweep signals from input syncs to provide 525 to 1023 line television raster.

3. Vertical Deflection/Sweep Fail Module - Generates the 60-Hz vertical deflection signal from input syncs. Also senses sweep failure and blanks display to prevent CRT damage.

4. Dynamic Focus/Horizontal Linearity Correction Module - Provides dynamic CRT spot focus signal as a function of the beam deflection position. Also provides correction function to insure linear deflection over the entire display.

5. High Voltage Power Supply - Generates all CRT and video amplifier voltage forms. Anode voltage adjustable from 15 KV to 20 KV depending on CRT.

6. Low Voltage Regulator - Regulates voltage from power transformer and rectifiers which are discrete components mounted on chassis. The module can also be used in Digital Signal Transfer Unit.

7. BIT Generator/Data MUX - Generates internal test pattern for display in CRT. Module outputs are checked, failure detections are made available on DAIS interface bus.

1.3.4 Multi-Mode Display Unit Special Module

CRT - Potted CRT assembly with magnetic deflection yokes. Size depends on application.

1.4 System Applications

The MMSDS design was applied to several avionics systems to determine the number of "core" and "special" modules required in each system. The results of this analysis is tabulated in Table 3. Each system uses all eleven types of core modules and various number of memory modules depending on the resolution requirements. The F-111 systems require two complete digital scan converter channels and therefore require approximately twice as many logic and memory modules as single channel systems. The "special" modules are primarily interface modules to convert the input data formats to compatible digital data word formats.

TABLE 3. MODULAR APPLICABILITY SUMMARY TABLE

Aircraft	Digital Signal Transfer Unit				Multi Mode Display		
	Core Modules	Memory Modules	Special Modules	DSTU Total	Core Modules	Special Modules (CRT Only)	Total Modules
F-4 (C, D & E)	13	4	4	21	16	2	18
F-106	13	2	3	18	8	1	9
A-7	13	4	5	22	8	1	9
F-111 (A, D, FB-111 & B-1)	26	9	8	43	16	2	18
B-1 EAR	26	26	3	55	16	2	18
F-15	13	2	2	17	8	1	9

A study was made of the application of the MMSDS to the A-7 avionics sensor system with a DAIS type interface. Four alternate display systems including an analog scan converter system, discrete digital system and both an LSI and MSI modular system were compared. The analog system included both an analog scan converter and symbol generator. The discrete digital design was an optimal digital design to meet the requirements of the specific A-7 application. The LSI system was the modular design partitioned on large 2.2 inch diameter bipolar IC wafer and hybrid circuitry modules. The MSI design was the same design mechanized with MSI and SSI integrated circuits mounted on printed circuit card modules. A detailed cost of ownership analysis of the alternates was conducted whereby the cost components were identified. A reliability analysis was also conducted. Both the LSI and MSI

modular signal transfer units and display indicators are physically described. The results of this trade-off study are summarized in Table 4.

TABLE 4. SUMMARY TRADEOFF TABLE ALTERNATE A-7/DAIS DISPLAY SYSTEMS

	Analog System	Discrete Digital System	Modular MSI	Modular LSI
Number of Modules	N.A.	29	34	28
Weight, lbs	65	45	47	40
Volume, cu ft	1.25	0.7	0.7	0.7
Power, watts	290	350	403	403
MTBF, hrs	190	765	670	1890
MTTR, hrs	4	1	0.5	0.5
Maintenance Adjustments	41	6	6	6
Relative Cost of Ownership (1st System)	1.7	1.0	1.1	1.0
Delta Cost (2nd System)	1.7	1.0	0.8	0.7
Delta Cost (3rd System)	1.7	1.0	0.7	0.6

1.5 Conclusions and Recommendations

The cost analysis of the modular system indicates a total program savings which increases with each successive system procurement using the modular design concept. These program savings can be further increased with improvements in maintenance and spares provisions that take advantage of the use of standard modules in different avionics systems. A key feature that contributes to the cost savings is LSI implementation of the "core" modules. The higher reliability and lower production cost of LSI leads to a significant program savings in mulitple system buys where the LSI development cost can be amortized over several systems. A second key feature of the modular system concept is the use of a programmable microprocessor to control the scan converter and symbol generator functions. This enables adaptation of the modular display system to different avionics system by simply reprogramming the microprocessor controller.

A two step development of the modular multi-sensor display system (MMSDS) is recommended. The first step would be the design and fabrication of an exploratory development model (EDM) utilizing discrete SSI and MSI digital logic elements but partitioned into LSI compatible functional modules. This EDM would serve as a vehicle to test and demonstrate the modular concept and to evaluate programming functions for the microprocessor controller. Alternate memory sizes could be mechanized to demonstrate various resolution systems and the microprocessor could be reprogrammed to demonstrate and evaluate the flexibility of the design. It would also provide the basis for the second stage of development; the design and fabrication of LSI and hybrid modules. This LSI development could be oriented towards fabrication of the "core" modules or towards fabrication of a production system for a specific aircraft application.

2.0 DETAIL MODULE DESIGN

2.1 Introduction

This section presents the design of the various system modules which constitute the signal transfer unit and display unit of the modular multi-sensor display system. Basically, the signal transfer unit consists of the digital scan converter and symbol generation functions. The actual design to meet the requirements is a multi-step process consisting of functional design, circuit design, physical module design and partitioning of the circuit design into modules.

The functional design is presented in this section in the form of a block diagram derived from the Functional Requirements, Design Performance Criteria, and Design Study sections of this report. The basic requirements are summarized in Table 5. A description of the basic core functions required in virtually all applications, follows the functional block diagram. These functions include A/D conversion, radar video processing, sensor data and symbol generator control, display refresh memory, clock generation and output video D/A conversion.

A summary of the functional circuit mechanization parameters is then presented. This summary includes the number of components, power, speed and interface requirements of the circuit mechanization necessary to provide the basic core functions.

Two alternate module physical configurations are described. They include a 5.6 x 6.2 inch printed circuit card module capable of holding up to 60 integrated circuits and a 4.1 x 4.6 inch LSI module. The LSI module is capable of replacing up to 80 integrated circuits.

Two alternate partitioning configurations are described, one using MSI components mounted on printed circuit boards and the second using LSI modules.

A description of all the core modules (12 LSI modules, 16 MSI modules) is presented along with a logic level schematic, interface definition and power estimate for each module.

The major emphasis in this study is on the core modules that make up the digital signal transfer unit (scan converter and symbol generator). However, five special modules which are uniquely required for specific applications are discussed. These are the interface modules, special purpose clock generator, out-of-scan-blanking module, and two video processing modules; a histogram equalization and video aging module. At the conclusion of this section, a modular display indicator unit consisting of 9 display modules is described.

TABLE 5. FUNCTIONAL REQUIREMENTS

General

- Radar Scan Conversion and EO Freeze Capability
- Symbol Generation Capability
- Maximum Use of Digital Components
- Multi-System Applicability
- Performance Modification by a Minimum of Hardware Changes
- Design Minimum Number of Core and Special Modules
- TV Monitor with Variable Line Rate

Modes

- Radar
  - PPI
  - Sidelooking Strip Mapping
  - Air-to-Ground Ranging
  - B-Scan
  - TF
- Electro Optical
  - IR Search and Track
  - EO Line Scan
  - TV Freeze

Parameters

- Digital Signal Transfer Unit

Input Interface	Analog Video from Sensor Control with DAIS, parallel data or existing system interface

(Continued next page)

(Table 5, continued)

A/D Converter	4 bit – 40 MHz (expandable to 6 bits)
Input Processing	Integrator, Truncator, Peak Detector
Integrator Length	2048 elements in range
Dynamic Range	12 bits (4096 intensity levels)
Feedback Ratio	1/2 to 31/32
Speed	Up to 10 MHz
Memory	
Size	256 x 256 x 1 (also 128 x 512) Bit incrementally expandable up to 1024 x 1024 elements of 12 bits each
Type	4096 Bit P or N channel MOS RAM
Speed	400 nsec cycle
D/A Converter	6 Bit 40 MHz
Symbol Generator	Chain type programmable
Output Processing	Video Mixing, Gamma Shaping and Rolloff filter
Control	
Architecture	Special Purpose Scan Converter and Symbol Generator Programmable Controller
Speed	250 nsec cycle
Word Length	16 Bits
Output Interface	Composite Video per EIA STD RS 170 and RS 343

- Display

Input Interface	Composite Video per EIA STD RS 170 and 343

(Continued next page)

(Table 5, concluded)

Format	525 to 1023 Line horizontal 2:1 Interlaced Raster
Bandwidth	±1 db to 30 MHz
Size	6 to 12 inch Diagonal to provide ~100 picture elements per inch
Phosphor	Green (such as P31 or P44)
Spot Size	<10 mil

2.2 Functional Description

A functional block diagram of the digital scan converter and symbol generator is shown in Figure 2. This system converts the input radar video to a television format and generates the required symbology in a television format. The design tradeoffs which resulted in this particular scan converter and symbol generator architecture are documented in Section 4.0 of this report. The programmable nature of the symbol generator makes possible the generation of the diverse shapes and combinations of symbology displayed in various aircraft. The output video, in a composite TV format can be displayed along with electro-optical sensor video on a standard TV monitor. It also can be recorded with a standard video recorder. Input control signals from a serial digital data bus are latched and converted to parallel control signals in a Subsystem Interface Unit (SSIU). The SSIU and Data Bus are elements of the Air Forces DAIS concept. The SSIU, and video recorder are not considered part of this design study. The purpose of each of the core functions are discussed in the following paragraphs.

Receivers. This function receives video signals from all sensors, switches to the appropriate video input (depending upon mode), and translates or scales the input voltage levels (of video and syncs) to those suitable for the internal circuits. Analog receiver, analog voltage scaler, digital data selector, and digital voltage scaler circuit functions are required.

A/D Converter (4 Bits). The analog to digital converter is required to encode the analog video sensor signals from the receivers into digital words for storage in the digital memory. Analog circuits, digital circuits, and passive components are necessary to provide the comparator, encoder, and ladder network functions of the A/D converter. In addition analog amplifiers, analog comparators, and passive components are required to implement the sample and hold input function that is necessary to assure valid digital outputs of the A/D.

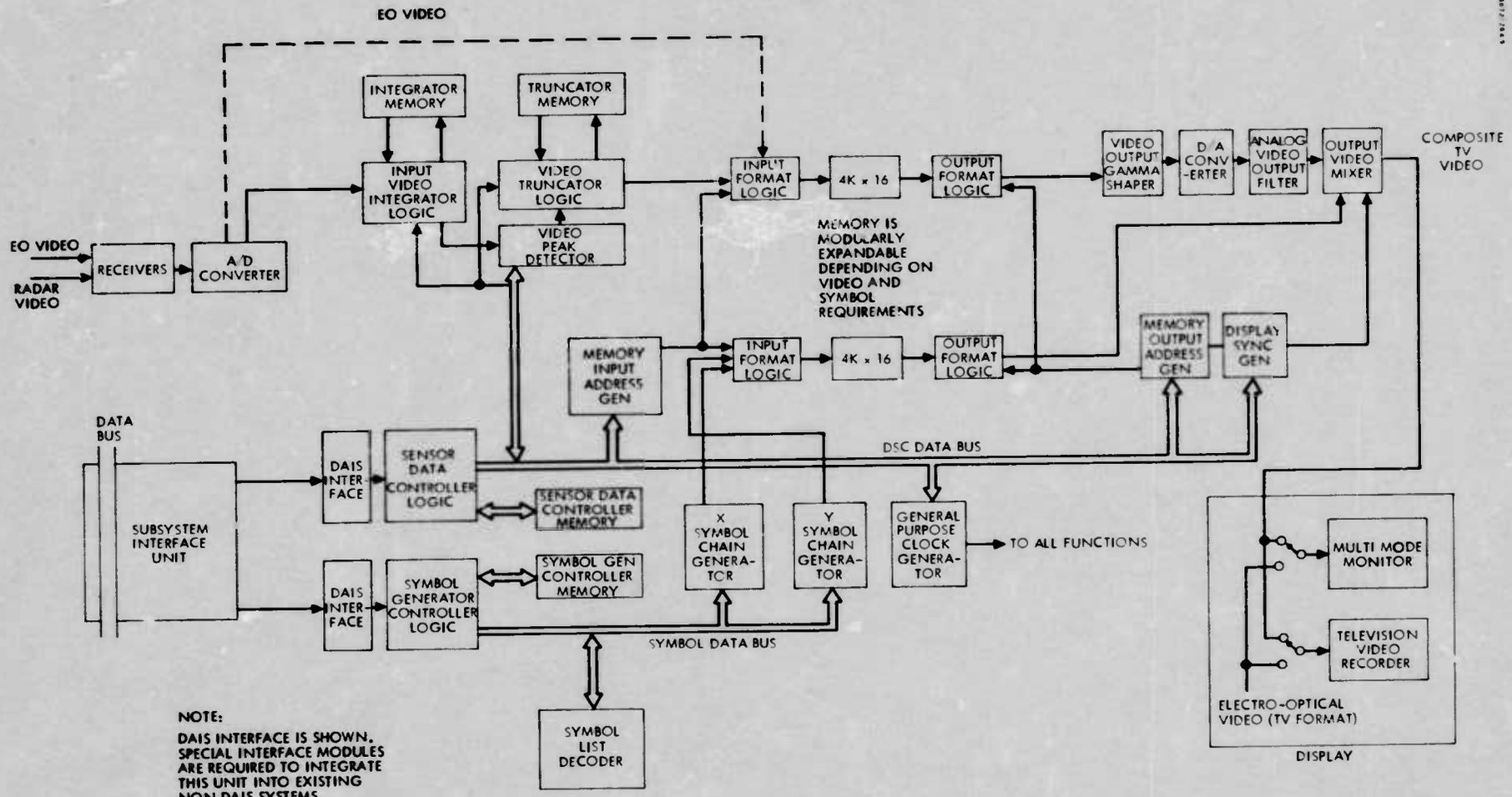


Figure 2. Modular display system functional block diagram.

Input Video Integrator. The integrator's function is to collapse the forward scanning input sweeps into the number of sweeps stored in the main memory as dictated by the resolution requirements. A digital adder, random access memory, and feedback logic are needed to implement the addition, sum accumulation, and feedback multiplication functions respectively.

Video Peak Detector. As the name implies, the peak detector selects the peak video from a series of video signals sent by the input video integrator. Digital logic circuits consisting of storage registers and comparators are required for implementation.

Video Truncator. The video truncator performs the necessary truncation of the accumulated sum from the input integrator (via the peak detector) upon its transfer to the display refresh memory. The specific truncation algorithm is under control of the sensor controller. Digital logic circuits such as counters, multiplexers, and random access memories must be provided to implement the required circuit functions.

DAIS Interface. This unit provides a system control function interface that utilizes the multiplex data bus technique characteristic of the DAIS concept for future aircraft systems. Digital logic circuits in the form of storage registers are required to receive mode and data information and transmit BIT (built-in-test) data via the subsystem interface unit according to the DAIS concept.

Sensor Data Controller. The purpose of the sensor data controller is to provide the basic scan converter and display timing signals for sampling the sensor inputs, commutating the input data in preparation for memory insertion, incrementing the memory input address generator, controlling the memory read cycle, and multiplexing the memory outputs. Digital data registers, arithmetic logic units (ALU's), counters, multiplexers, and read only memories (for storing program and constants) are the circuit elements necessary to implement the required functions.

Symbol Generator Controller. The function of the symbol generator controller is to provide timing and control signals for symbol generation. The digital circuit functions that are required are data storage, ALU's, counters, data selectors, read only memories (for holding program), and random access memories (for compiling display lists).

Memory Input Address Generator. The purpose of this function is to control the memory address during data insertion so as to place the incoming sensor video data in its proper location. The input addressing scheme must have the flexibility to transform all sensor scan patterns to TV raster format. Counter, data storage, and rate multiplier digital circuit functions are required.

Memory Input Format Logic. The input format logic commutates or demultiplexes the input data from the truncator for insertion into the memory. Digital logic circuits consisting of serial to parallel shift registers and buffer registers are required to implement the circuit functions.

Display Refresh Memory. The function of this memory is to store an entire image of sensor and symbol data for rapid refresh of the CRT display. The digital circuit functions required are RAMs, logic level translators, and clock drivers.

Memory Output Format Logic. The output format logic multiplexes the multiple memory output lines down to a smaller number of bits suitable for D/A conversion. A parallel to serial shift register is the primary digital circuit function utilized.

Memory Output Address Generator. The purpose of this function is to control the read memory address sequence. By using a TV raster format for the display the read address sequence becomes a counting function. Accordingly digital counter circuit functions are required for implementation.

Display Sync Generator. This function generates the horizontal and vertical syncs and blanking signals for the CRT display. Digital data storage, rate multiplication, and counting circuits are necessary to implement the required functions.

Video Output Gamma Shaper. The purpose of the gamma shaper is to match the video intensity function to the brightness transfer function of the CRT display so that linearity is achieved. Digital storage register and read only memory circuits are necessary to implement the required functions.

Video Output D/A Converter. This function converts the digital video code from the memory output format logic to a video analog signal suitable for display on a CRT monitor. A resistor ladder network and an analog amplifier are necessary to provide the required circuit functions.

Analog Video Output Filter. This function's purpose is to smooth the video output signal from the D/A converter for providing a more pleasing display. Passive circuit components and an analog amplifier are necessary to implement the circuit functions.

Output Video Mixer. This function combines sensor video data with symbol video data and mixes in horizontal and vertical syncs to form a composite video signal meeting EIA standards for the CRT display. Passive circuit components and an analog amplifier must be provided to satisfy the circuit function requirements.

General Purpose Clock Generator. The clock generator provides all scan converter and symbol generator clock signals for the system. It includes digital storage register, counter, comparator, and control flip-flop circuit functions in addition to D/A converters and voltage controlled oscillators.

Symbol Chain Generator. The symbol chain generator is responsible for the generation of the x and y symbol addresses. Digital circuit functions such as storage registers, adders, and multiplexers are required for implementation.

Symbol List Decoder. This function decodes the symbol list generated by the symbol generator controller to form the chain generator controls and chain data. Digital circuits consisting of storage registers, counters, and combinational logic are necessary to implement the required functions.

2.3 Summary Detail of Function Mechanization

The logic design of the functions described was conducted based on the mechanization parameters derived in Section 3.0 (Volume I). A summary of this design is presented in Table 6 listing the parameters required to perform the partitioning task. The number of integrated circuits, input/output pins, circuit speeds and total power for all of the functions which constitute the Digital Signal Transfer Unit core modules are presented in this table.

2.4 Module Physical Description

2.4.1 MSI Module

Figure 3 shows the basic card module selected for the MSI modular display system. This is a multi-layer printed circuit card with single side component mounting and measures 5.6 inches wide by 6.25 inches high by 0.38 inch maximum thickness, including the card connector. This card size is optimum because (1) it's compatible with many different aircraft applications including F-4, A-7, F-111 and F-106, and (2) it can accommodate a sufficient number of components for optimum partitioning. It will carry up to 60 IC packages, dual-in-lines (DIPS) and/or flat packs, along with an adequate mix of other components such as transistors, diodes, capacitors and resistors. Up to one hundred (100) input/output contacts are available on each card module, and it is small enough to avoid vibrational problems.

This card is capable of dissipating twenty watts with convection cooling under worst case conditions when the system is in the cockpit compartment without aircraft supplied cooling air. Proven computer routing programs are currently available for this card module.

TABLE 6. DIGITAL SIGNAL TRANSFER UNIT DESIGN SUMMARY

Functional	I/O Signals	Number of IC's	Power, w	Voltages	Circuit Relative Speed, MHz	
Video and Sync Receivers	47	36	3.8	±15, +5	10	
Analog to Digital Converter	7	19	5.5	±15, +5, -5.2	90	
Input Video Integrator	50	62	22.7	+5	10	
Video Peak Detector	38	12	3.0	+5	10	
Video Truncator	40	17	4.3	+5	10	
DAIS Interface	36	7	1.34	+5	4	
Sensor Data Controller	84	55	11.3	+5	4	
Symbol Generator Controller	84	55	11.3	+5	4	
Memory Input Format Logic	50	20	5.0	+5	40	Quantities Listed per 4K x 16 Module
Display Refresh Memory	25	24	7.2	+12, +5, -3	40	
Memory Output Format Logic	42	9	1.3	+5	40	
Memory Input Addressing Logic	62	47	8.5	+5	10	
Memory Output Address Generator	51	14	3.8	+5	10	
Display Sync Generator	32	10	3.6	+5	10	
Video Output Gamma Shaper	39	15	1.8	+5	10	
X Symbol Chain Decoder	36	31	5.6	+5	5	
Y Symbol Chain Decoder	36	31	5.6	+5	5	
Output Digital to Analog Conv.	16	18	1.0	±15, +5	10	
Analog Video Filter	16	8	0.8	±15, +5	20	
Output Video Mixer	23	8	1.5	±15, +5	10	
Symbol List Decoder	80	75	14.0	+5	4	
Sensor Data Controller Memory	71	10	6.8	+12, +5, -3	4	
Symbol Generator Controller Memory	71	34	17.4	+5	4	

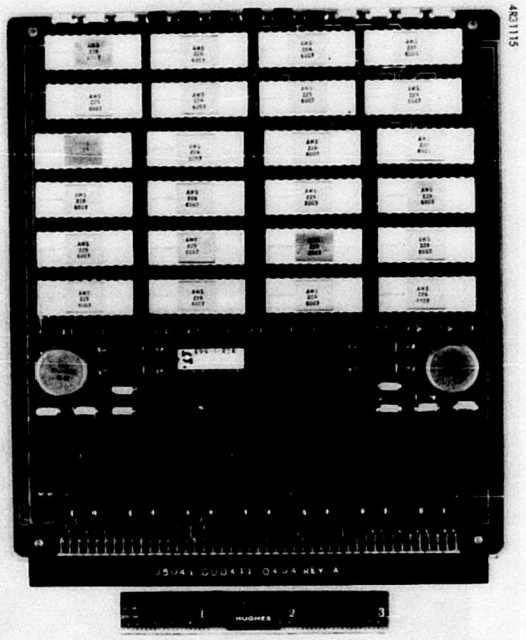


Figure 3. Typical card module.

2.4.2 LSI Module

Figure 4 shows the LSI wafer card module assembly selected for the modular display system. It measures 4.7 by 4.1 inches by 0.43 inch. It consists of a ceramic package, a metal heat exchanger bonded to the back of the package, an etched circuit board to provide inter-connections down the back side of the module, a "crossover comb" spanning the top of the module to interconnect the top of the substrate to the etched circuit card, and a structural frame with air in-out slots.

The hollow-core heat exchanger will have a lanced-offset channel configuration that has been proven to be more effective than a straight channel configuration. The card module "plugs in" to the unit card rack and utilizes direct cooling from the unit air supply.

The module is based on the use of the Hughes 2.2 inch diameter Bipolar Pad Relocation LSI wafer. PAD relocation LSI is a means developed by Hughes of using multi-layer wafers to interconnect a standard set of operational circuits. The advantage of this approach over custom LSI is twofold. First, standard wafers can be designed with a logic "mix" which maximizes it applicability. Secondly, the LSI yield is increased since only operating

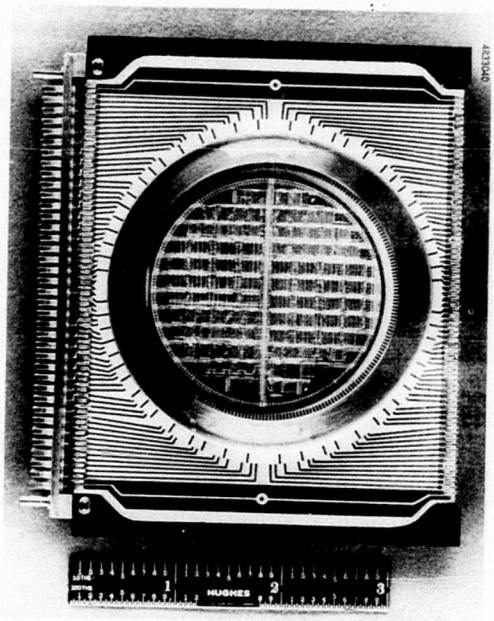


Figure 4. Full wafer LSI array module.

circuits are interconnected. A complete description of Hughes Pad Relocation LSI is presented in Appendix A. The basic wafer can replace the equivalent of up to 80 integrated circuits (depending on complexity) and can dissipate up to 20 watts. The selected module has 144 I/O pins.

The pad relocation LSI wafer replaces random bipolar logic implemented with SSI and MSI components. However, it is not applicable to linear analog circuits such as required in the input A/D converter and output D/A conversion. It is also not applicable to memory (both ROM and RAM). Therefore, to provide maximum large scale integration, hybrid modules are recommended to provide these functions. A basic hybrid module with two hybrid circuits and miscellaneous discrete integrated circuits is shown in Figure 5. It is the same size as the LSI wafer module (4.1 x 4.7 inches) with 144 I/O pins and will dissipate up to 25 watts.

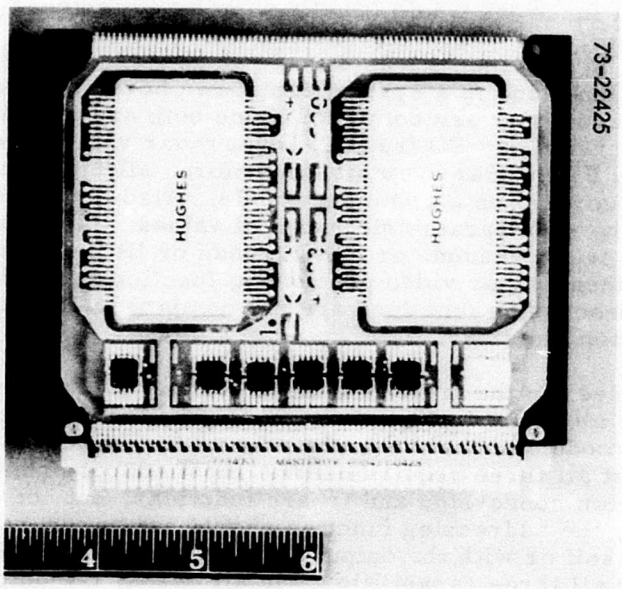


Figure 5. Two Hughes one by two inch hybrid packages mounted on module.

2.5 Module Partitioning

The partitioning of the design into modules is an iterative process, trading off the physical constraints against the functional preferences. Two alternate partitioning designs were conducted for this study. One used MSI circuitry and the other used LSI circuitry.

Functionally it is desirable to partition the circuitry (functions) into modules that maximize multi-system applicability and flexibility. One rationale used in this study was to group basic functions that are always used together on a common module. Also, functions that interface with each other were grouped together to minimize the number of system interconnections. This functional partitioning criteria is best illustrated by Table 7 which summarizes three basic display system functional capabilities: radar scan conversion, electro-optical video storage, and symbol generation. For display systems, these capabilities can either be individually provided or any possible combination of them can be used. The table not only indicates what system functions are applicable for each system capability but also specifies what functions would benefit from being included on the same module.

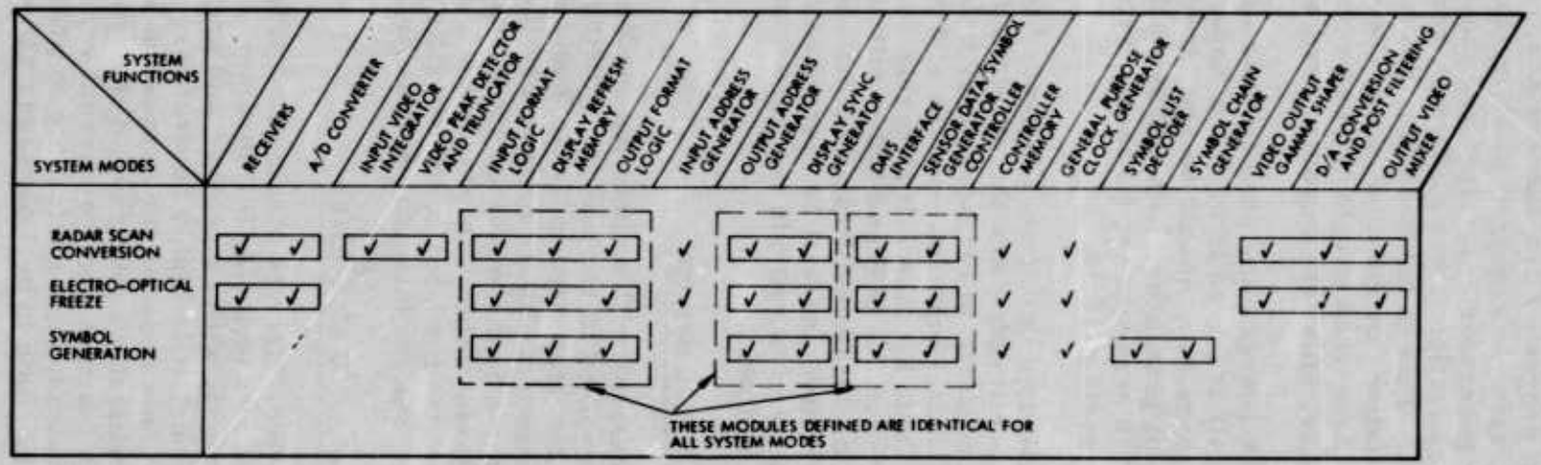
The major functions in a system are shown horizontally. The video receiver and A/D converter are combined since both are required together for both scan conversion and EO freeze. Input radar video processing is required in the low PRF radar systems, therefore, all these input processing functions are provided on a common module. Also, the module must be designed to meet the wide parametric range of values. In systems where the radar video is preprocessed, or if EO freeze or IR line scan conversion only is required, these radar video processing functions are not required, therefore, those processing functions are not combined with the memory or input A/D conversion functions.

As can be seen in the table, all three system capabilities require memory and some means of input and output format logic. Therefore, a common memory module should be designed with the input and output format logic that will meet all three requirements. Input address generation is required for the scan conversion and freeze functions, but not symbol generation. Therefore, the addressing function should not be incorporated on the memory module itself or with the output address generation function since these are used for all three capabilities. In all cases, the output memory addressing is required and so is display sync generation therefore these functions are incorporated in the same module. The same basic digital counters can then be used for both the address and sync generation.

The controller design is used for control of scan conversion, EO freeze and for symbol generator control. It utilizes a parallel digital control interface which is basically the way data comes from the Subsystem Interface Unit of DAIS. Therefore, this interface should be included on the controller

TABLE 7. FUNCTIONAL PARTITIONING FOR THE MODULAR DISPLAY SYSTEM

The system functions that are appropriate for each system mode are checked. The heavy lines surrounding certain system functions indicate that it is desirable to include these functions on the same module if possible to achieve a more efficient system partitioning.



module. In addition to the controller, a memory is required which stores the basic system programs and subroutines. A general purpose programmable clock generator is required in all systems. Since the output address generator, sync generator controller and clock generator are all used together in all applications, it would seem reasonable to put them together in the same module. This is not possible, however, due to their complexity and the physical limitations of the modules. The controller memory should have its own separate module since if it becomes necessary to reprogram or modify the system parameters, only this (module) need be removed from the system.

Video D/A conversion, gamma shaping, post filtering and video and sync mixing are all required in both the Radar Scan Converter and EO freeze system, therefore, should be combined in the same module. In the area of the symbol generator, both the symbol list decoder and chain generator are required to generate the in-raster symbology and logically should be combined on the same module.

As previously mentioned, the second important criteria required to achieve the LSI partitioning are the physical design guidelines. Particularly, the design must conform to the previously defined limitations regarding the complexity (# circuits) input/output pins and power. These criteria are summarized in Table 8. Also, it is highly desirable to maximize module commonality between the MSI and LSI partitioned systems. The MSI system will most likely be developed first, but the LSI partitioning criteria are much more restrictive and will be discussed first. A discussion of the exceptions to be taken to provide the core modules compatible with the MSI design will then follow.

2.5.1 LSI Partitioned System

This discussion will include the fundamental tradeoffs and design considerations involved in the LSI partitioning process and will reflect the system information presented in Table 7 and 8. The specific system partition derived is shown in Figure 6, in which the module definitions have been superimposed on the Scan Converter functional block diagram presented earlier. In addition, Table 9 is presented to summarize the partitioning results and relate the modules to the specific forms of LSI required for implementation. The module and package definitions are discussed below.

Receivers, A/D Converter

The Receiver circuits obtain input video signals from all sensors and transfer their outputs to the A/D Converter. Since these functions always communicate directly with each other and are always required together in system applications, it is highly desirable to include them on the same module if possible. This reduces the number of intermodule interconnects and thus improves reliability. Because of the types and amount of circuitry required by each function and the current availability of a previously designed A/D converter hybrid, it is preferable to provide separate hybrid packages for each function. Both hybrid packages can easily be accommodated by a single module.

TABLE 8. PARTITIONING CRITERIA

The partitioning of a system requires both functional knowledge of the system and recognition of the characteristics and constraints of the physical module limitations.

System Related Factors

Preservation of natural divisions

Maintenance of functional continuity

Minimization of number of modules

Minimization of number of module types

Prevention of test difficulties

Module Physical Related Factors

Factors	MSI	LSI	
		Bipolar	Hybrid
Minimization of I/O's	100	144	144
Module Size	5.6 x 5.9	4.7 x 4.0	4.7 x 4.0
Power dissipation capability	25 W	20 W	25 W
Maximum circuit complexity	60 IC	approx. 80 IC	–

Input Video Process Logic Module

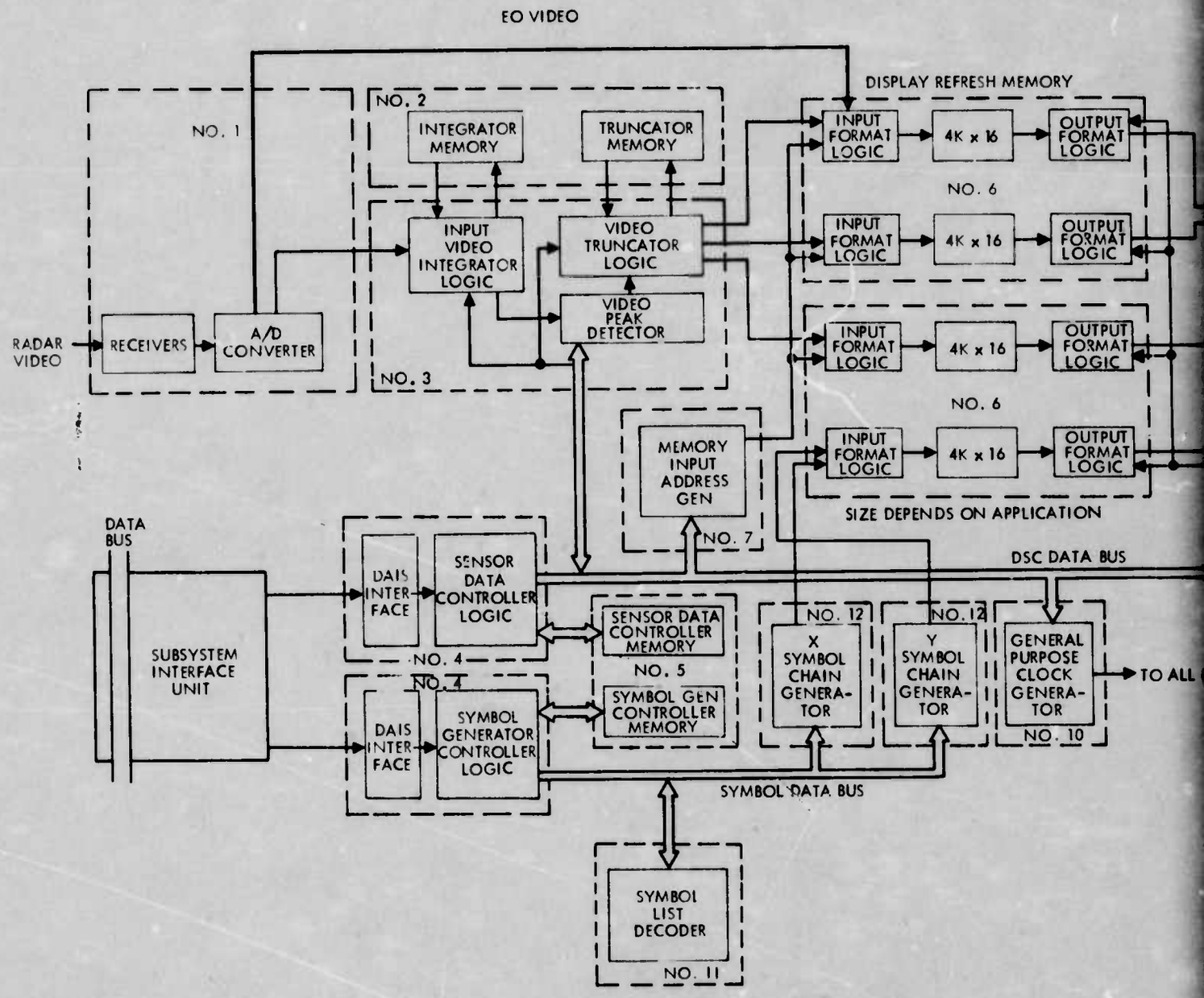
All input radar video processing functions should be included in the same module because the use of one requires the use of all. These functions are the Input Video Integrator, Video Peak Detector, and Video Truncator. All functions must be implemented with digital circuits and a large portion of the digital logic requirements can efficiently be satisfied by full wafer LSI. However, portions of the integrator and truncator functions have data storage requirements necessitating memory devices. Full wafer LSI implementation of memories is currently not available. Accordingly, a hybrid memory package is placed off the full wafer LSI module due to practical packaging limitations (forming a separate hybrid module). The remaining random logic requirements of the functions can be efficiently satisfied with one full wafer LSI array that will comprise a module. Thus an efficient implementation of the functions is realized by trading off functional characteristics and LSI design requirements.

Main Memory Module

The Memory Input and Output Format Logic functions are always required with the Display Refresh Memory in all systems. These functions also communicate directly with the Memory. Thus, it is desirable to include these functions on the same modules. This not only preserves the functional boundaries of the system but also reduces the number of inter-module interconnections. The digital logic functions of the Input and Output Format Logic can be efficiently implemented with LSI arrays. To reduce the number of module I/Os required a bit slice partitioning of the memory was conducted to provide both the scan conversion and symbol refresh functions. Practical packaging guidelines, and a study of system memory requirements indicates that 64K bits of memory organized 256 X 256 X 1 with input and output format logic is a reasonable memory configuration. Two such arrays can be placed on two sides for the module. Thus each module side will contain a memory hybrid package and a partial wafer LSI package for the Format Logic. The amount of Format Logic associated with each of the four Memory segments is not enough to necessitate a complete full wafer LSI array. The Memory and Format Logic packages on each module side communicate using interconnections provided on the PC board.

Memory Input Address Generator Module

The Memory Input Address Generator function is used in the electro-optical and radar scan conversion systems. This system function consists of strictly digital functions that can be satisfied with the logic circuits provided by full wafer LSI. The allocation of a separate module for this function is warranted because it conforms to the natural system functional boundaries and contains an appropriate amount of logic for a full wafer LSI array. Thus, a module containing a full wafer LSI array is recommended.


EO VIDEO
DISPLAY REFRESH MEMORY
NO. 1
NO. 2
INTEGRATOR MEMORY
TRUNCATOR MEMORY
INPUT VIDEO INTEGRATOR LOGIC
VIDEO TRUNCATOR LOGIC
VIDEO PEAK DETECTOR
NO. 3
RADAR VIDEO
RECEIVERS
A/D CONVERTER
INPUT FORMAT LOGIC
4K x 16
OUTPUT FORMAT LOGIC
NO. 6
NO. 6
SIZE DEPENDS ON APPLICATION
MEMORY INPUT ADDRESS GEN
NO. 7
DATA BUS
SUBSYSTEM INTERFACE UNIT
DAIS INTER FACE
SENSOR DATA CONTROLLER LOGIC
NO. 4
SENSOR DATA CONTROLLER MEMORY
NO. 5
SYMBOL GEN CONTROLLER MEMORY
NO. 4
DAIS INTER FACE
SYMBOL GENERATOR CONTROLLER LOGIC
DSC DATA BUS
NO. 12
X SYMBOL CHAIN GENERA-TOR
NO. 12
Y SYMBOL CHAIN GENERA-TOR
GENERAL PURPOSE CLOCK GENERA-TOR
NO. 10
TO ALL
SYMBOL DATA BUS
SYMBOL LIST DECODER
NO. 11

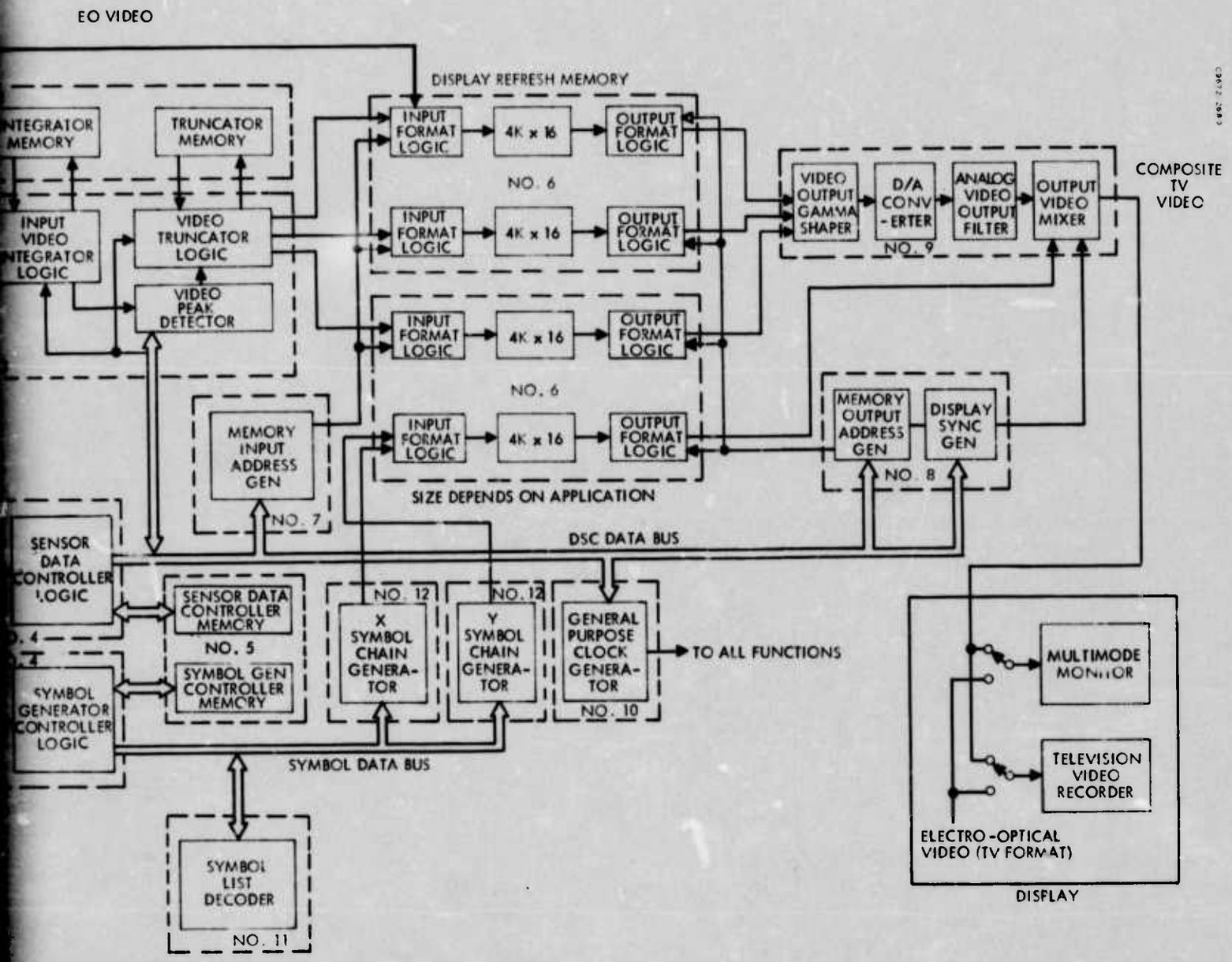


Figure 6. LSI partitioned modular display system.

Module		Hybrid Packages/Module			LS	
Identification Number	Designation	Number per Module	Type	Designation	Number per Module	T
1	Receivers, A/D Converter	1 1	Linear Linear	Receivers A/D Converter		
2	Input Process Memory	1	Memory	Integrator and Truncator Memory		
3	Input Video Process Logic				1	Full
4	Sensor Data and Symbol Generator Controller				1	Full
5	Sensor Data and Symbol Generator Controller Memories	1 1	Memory Memory	Sensor Data Controller Memory Symbol Generator Controller Memory		
6	Display Refresh	2	Memory	Display Refresh Memory	2	Par Waf
7	Memory Input Address Generator				1	Full
8	Memory Output Address and Display Sync Generators				1	Full
9	Output Processing	1	Mixed	Output Processor		
10	Clock Generator				1	Nea waf Spe Dev
11	Symbol List Decoder				1	Ful
12	Symbol Chain Generator				1	Ful

TABLE 9 SUMMARY OF LSI CORE MODULE PARTITIONING

LSI Wafers/ Module			Total Package per Module	Equivalent Number of ICS	Number of I/O	Power, W	Voltage Forms	Circuit Speed, MHz
Number per Module	Type	Designation						
			2	55	41	9	±15, +5, -5.2	10
			1	30	55	15	+5	10
1	Full Wafer	Input Video Processor	1	32	90	8	+5	10
1	Full Wafer	Sensor Data and Symbol Gen. Controller	1	62	66	14	+5	4
			2	70	104	24	+12, +5, -3	4
2	Partial Wafer	Input and Output Format Logic	4	106	28	27	+12, +5, -3	40
1	Full Wafer	Memory Input Address Generator	1	53	64	8	+5	10
1	Full Wafer	Memory Output Address and Display Sync Generators	1	42	46	8	+5	10
			1	14	26	3	±15, +5	10
1	Nearly full wafer Special Devices	Clock Generator	1	58	37	18	±15, +5	40
1	Full Wafer	Symbol List Decoder	1	76	82	14	+5	4
1	Full Wafer	Symbol Chain Generator	1	31	60	18	+5	4

Memory Output Address and Display Sync Generators Module

The Memory Output Address Generator and Display Sync Generator functions share the same clocking signals since they must be inherently synchronized. In addition there are no system applications that require only one of the functions (see Table 8). These functional considerations dictate that they should remain together if possible. Preliminary analysis of the digital logic requirements relative to the LSI guidelines confirmed that both functions can be implemented with a single full wafer LSI array. Accordingly, a module is defined which includes both functions and consists of an LSI array.

Output Processing Module

The Video Output Gamma Shaper, Video Output D/A Converter, Analog Video Output Filter, and Output Video Mixer are all considered output processing functions. The Gamma Shaper, D/A Converter, and Filter are always required in digital video systems driving a cathode ray tube display. At least one mixer channel is required since composite syncs must be mixed with the video. In some systems it is necessary to provide a second mixing channel for symbology. Thus it is desirable from functional and packaging efficiency standpoints to provide all of these functions with two mixing channels on the same module if possible. The requirement for a small number of digital and analog circuits necessitated the use of hybrids for an efficient implementation. It was determined that the total amount of circuitry required can be accommodated by one hybrid package. Thus a module containing a hybrid circuit implements all the desired functions.

Clock Generator Module

Input and output synchronizing clock signals as generated by the General Purpose Clock Generator function must be provided for several functional units of the system. In order to minimize noise it is desirable to minimize the number of clock sources by generating as many clock signals as possible from a basic centralized clock. For this reason as well as others such as preservation of system function characteristics and packaging efficiency, it is desirable to provide all clock generation functions on a single module. A review of the required circuit functions reveals that although digital circuits such as provided by full wafer LSI can satisfy most requirements, a small number of specialized analog devices are necessary. A special packaging technique is necessary to accommodate both types of circuits on the same module. Since the amount of digital logic does not require an entire full wafer for implementation, a small unused portion can be designated and removed from the rest of the wafer by dicing. The resulting space made available in the LSI package/module can be used for the placement, mounting, and interconnection of the special device chips. Thus an LSI module containing an LSI array and special devices within the same LSI package can fully implement all functions of the clock generator.

Symbol List Decoder and Symbol Chain Generator Modules

It is desirable to include the Symbol List Decoder and Symbol Chain Generator functions on the same module, since both must operate together to provide in-raster symbology. An analysis of the circuit requirements indicates that they are compatible with the digital circuit capabilities of full wafer LSI. In fact, three full wafer LSI arrays are actually necessary to accommodate the circuitry required for implementation of the two symbol generator functions. Thus the two system functions must be divided into three segments that may each be implemented with a full wafer array. To maintain system functional boundaries and minimize the number of inter-module interconnections the natural division between the Symbol List Decoder and Symbol Chain Generator should be preserved. Upon further analysis it was indicated that the Symbol List Decoder can be completely implemented with one full wafer LSI array. It was also noted that the Symbol Chain Generator contains two identical portions of circuitry for the generation of X and Y addresses. Each portion is suitable for an implementation with a full wafer LSI array. Although two full wafer arrays are required for the Chain Generator only one wafer type is required, thus realizing a significant cost saving. To summarize, a total of three LSI arrays of two types is necessary for the implementation of the Symbol List Decoder and Symbol Chain Generator.

Sensor Data/Symbol Generator Controller Modules

The DAIS Interface function provides a control function interface that receives and transmits data to units outside the Scan Converter. Inside the Baseline Scan Converter this function communicates directly with each of two system functions: the Sensor Data Controller and the Symbol Generator Controller. More generally, however, all combinations of these two functions will be utilized to satisfy various system requirements. The controller functions generate a variety of control signals for the other functional units of the system. These system functional characteristics make it very desirable to separate the two controller functions onto different modules while including the DAIS Interface with each. This reduces the number of inter-module interconnections while providing system flexibility and implementation efficiency. The arithmetic logic count and control portions of both the symbol generator and scan converter controller are identical and can be implemented on one LSI full wafer. Also, both the Sensor Data and Symbol Generator Controllers have a requirement for data storage. Separate memory hybrid packages are provided for the memory devices required. The separation of memory (ROM) also simplifies the reprogramming necessary to incorporate new modes or symbology. This is also desirable for efficient system implementation. When only one controller function is needed the hardware associated with the unused function is not included unnecessarily.

2.5.2 MSI Partitioned System

To provide the optimum MSI system partitioning the same basic ground rules were followed as in the case of LSI. The functional partitioning goals are exactly the same. However, due to the reduced packaging density, it was not feasible to accommodate the same amount of circuitry on the selected MSI circuit card module. The resultant MSI partitioned system is shown in Figure 7.

A study of the two block diagrams, Figures 6 and 7, reveals only slight differences in the partitioning. These differences all stem from the reduced packaging density of the MSI device implementation as compared to LSI. Extra modules are required for memory, controller, and clock generation.

The only difference in the area of the main memory is that one 256 x 256 x 1 bit channel is provided per module since the number of ICs required for two channels (106) exceed the MSI card limit of 60 ICs. The number of ICs in the controller itself exceeds the limit of 60, therefore some of the circuits will be relocated on the controller memory module. This results in overpopulation of the card, therefore the recommended partitioning is to provide separate controller memory modules; one for sensor data control and one for symbol generator control. The 78 integrated circuits required for clock generation cannot be provided on one module due to their complexity, therefore two modules are defined, one for input clocks and the second for output clocks.

Table 10 indicates the number of ICs, number of interconnects, speed, failure rate, and power of the resulting MSI partitioned core modules. The assumptions upon which the failure rates were computed are discussed in Section 3.5.

2.6 Core Module Description

The following is a description of the various core modules necessary to provide the scan conversion and symbol generation functions. These descriptions include interface definition, power requirements, clock rates and functional logic diagrams.

2.6.1 A/D Converter and Video and Sync Receiver Module

Module Requirements

The module provides video and sync receivers to accept differential or single-ended input, provide proper line termination, and isolation from ground. The sync triggering level shall be variable by Sensor Data Controller and convert the sync signal to TTL levels. Four to one multiplexing shall be provided for the receivers selectable by mode control. A sync stipper is provided for sync separation of composite syncs or video. A block diagram of this module is shown in Figure 8.

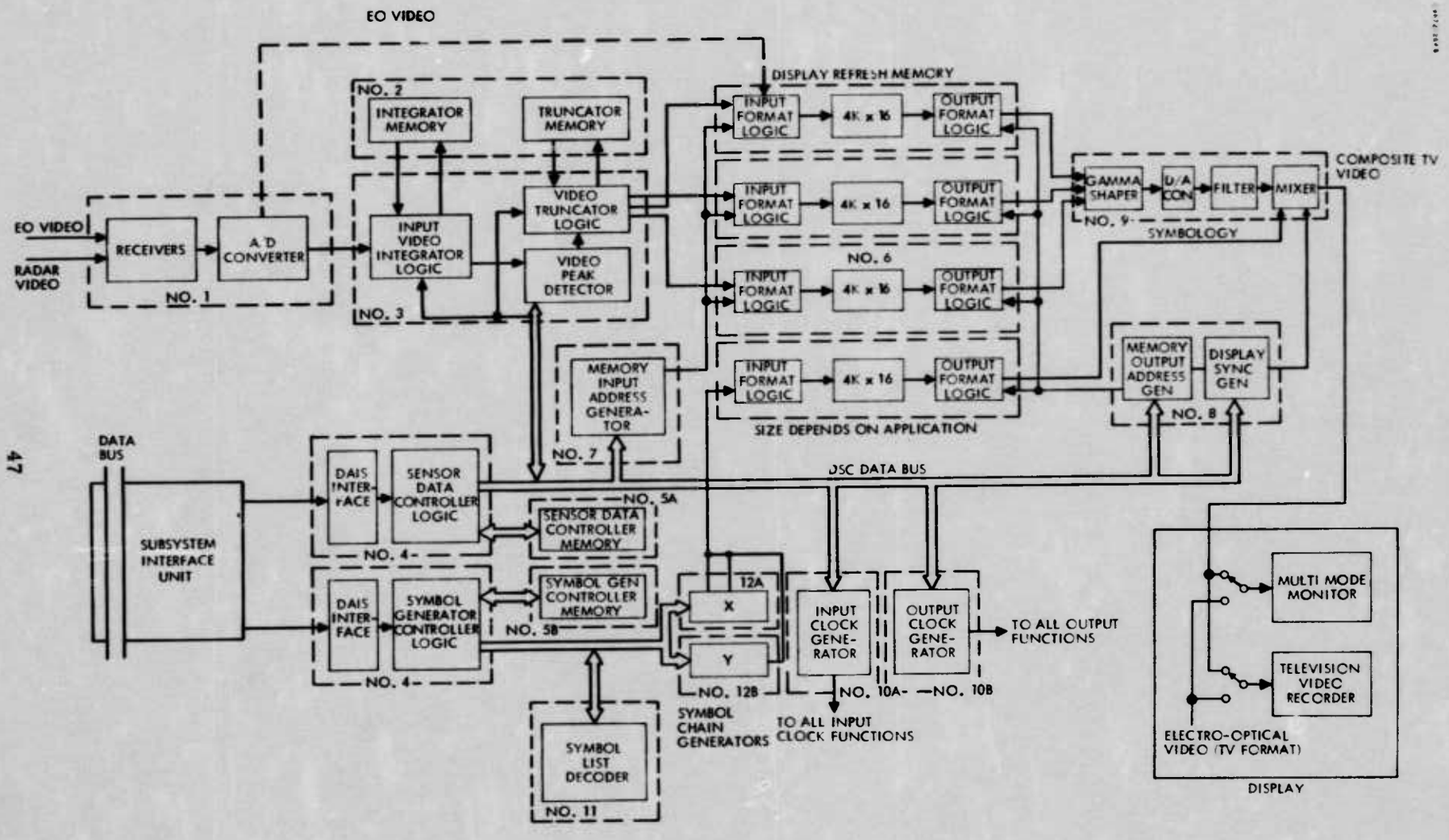


Figure 7. MSI partitioning of modular display system.

TABLE 10. SUMMARY OF MSI CORE MODULE PARTITIONING

	MSI	I/O	Number of IC's	Power, W	Voltages	Circuit Relative Speed, MHz	Failure Rates %/1000 Hrs
1	Receivers and A/D	42	48	9	±15, +5, -5, 2	10	2.6
2	Integrator and Truncator Memory	55	30	15	+5	10	1.7
3	Integrator, Peak Detect, and Trunc. Logic	92	39	8	±15, +5	10	2.2
4	Sensor Data and Symbol Controller and DAIS Interface	66	50	11	+5	4	2.8
5A	Sensor Data Controller Memory	52	23	10	+5	4	5.0
5B	Symbol Generator Controller Memory	52	47	20	+12, +5, -3	4	14.0
6	Display Refresh Memory	24	53	13	+12, +5, -3	40	9.0
7	Memory Input Address Generator	64	47	8	+5	10	2.6
8	Memory Output Address and Display Sync Generator	46	42	8	+5	10	2.3
9	Output Video Processing	26	36	3	±15, +5	10	2.0
10A	Input Clock Generator	31	29	4	±15, +5	40	1.6
10B	Output Clock Generator	31	29	4	±15, +5	40	1.6
11	Symbol List Decoder	57	50	10	+5	4	2.8
12A	X Symbol Chain Generator	88	49	9	+5	4	2.7
12B	Y Symbol Chain Generator	99	39	7	+5	4	2.2

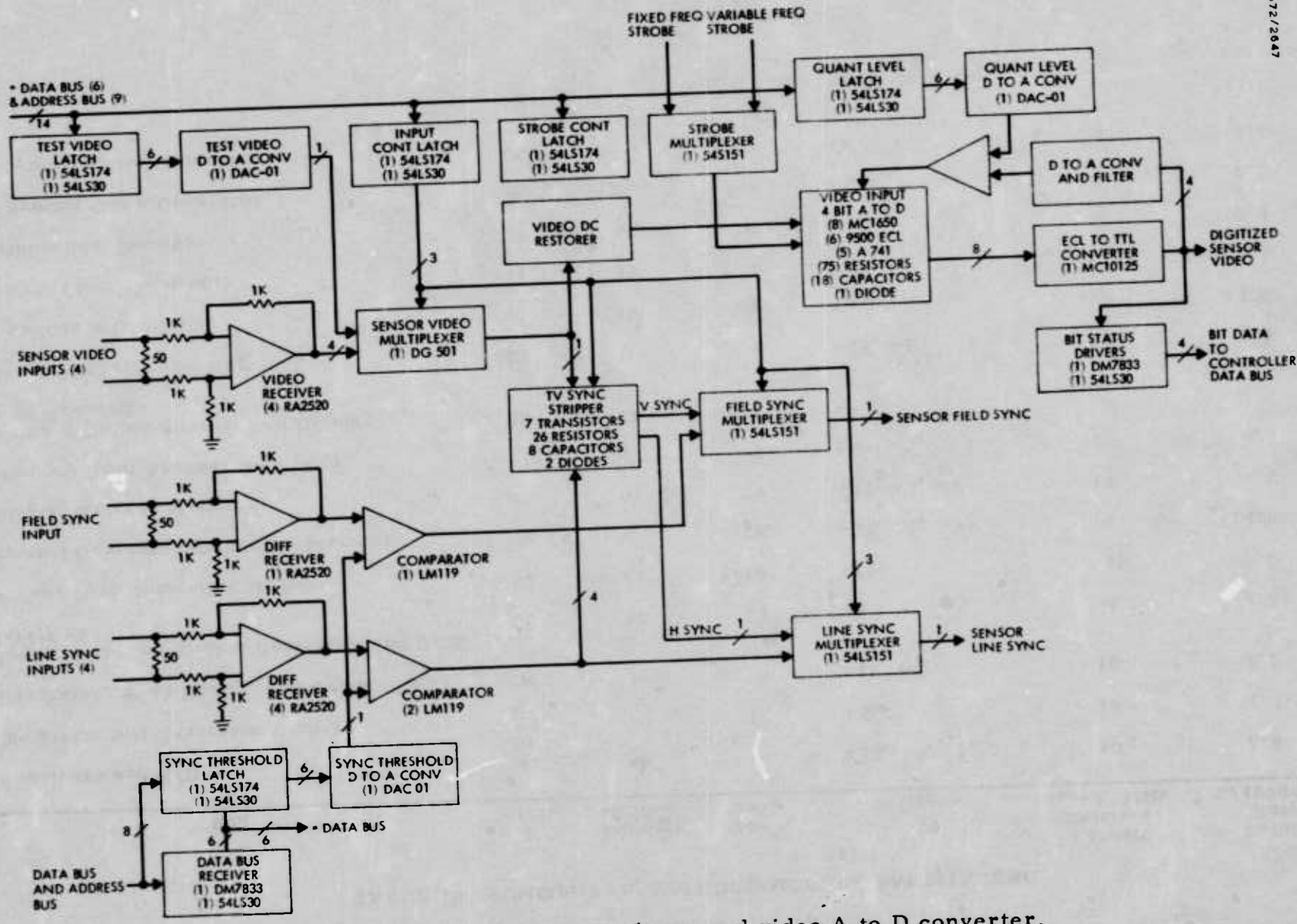


Figure 8. Video and sync receivers and video A to D converter.

An analog to digital converter shall be provided to digitize analog video up to 6 bits at a 40 MHz word rate. The A/D input voltage required for full digital scale variation shall be adjustable by Sensor Data Controller.

Signal	Number of Lines	Signal Type	Characteristics
Input Interface			
Input Video	8	Analog	20 MHz
Input Sync	8	Pulse	20 MHz
Data Bus	6	Tri State	1 MHz
Address Bus	9	Tri State	1 MHz
Field Sync	2	Pulse	60 Hz
Strobes	2	Pulse	10 MHz
Sync Threshold	1	Analog	DC Level (MSI only)
Output Interface			
Digital Video	4	TTL	40 MHz
Line Sync	1	TTL	50 KHz
Field Sync	1	TTL	60 Hz

Module Description

Video and Sync Receivers - The receiver circuits are needed to buffer the multiple sensor analog video inputs, sensor line sync inputs, and sensor field sync inputs. In addition, specific video and sync signals must be selected from the many buffered inputs by means of instruction codes from the sensor data controller function, for transmission to the other functions where they are needed. The receiver function has three data channels; the video channel, field sync channel, and line sync channel.

There are four analog video inputs to the video channel. Each video input circuit must provide a differential 50Ω line termination with a 2KΩ to ground impedance for each side of the differential pair. Four 20 MHz differential input analog amplifiers with high common mode rejection serve as the input buffers. The four buffered video signals are fed to an analog multiplexer circuit which selects one of the four video signals or a

built in test voltage for transmission to the analog to digital converter function. The analog multiplexer is controlled by the sensor data controller function by means of an instruction word which is sent over the system data bus and stored in a latch in the receiver circuits. All instruction words are updated whenever a mode change occurs. The DC analog test voltage is formed by a special low speed 6 bit digital to analog converter which is again set by an instruction word sent from the controller over the system data bus. The last circuit in the channel which is connected to the video output line is a discrete analog sync stripper used in the television modes. It separates the horizontal and vertical syncs from the composite TV video. The output of the line sync buffers are also fed to the sync stripper to separate the horizontal and vertical syncs when the composite TV syncs do not arrive mixed with the video.

The field sync channel contains one differential input receiver with input requirements identical to those of the video receivers. However, the receiver always uses an analog comparator to provide an adjustable threshold level which is controlled by an instruction word from the controller through a digital to analog converter. The receiver's output must be TTL compatible. The field sync is a low frequency signal but must be able to gate 40 MHz signals. The field sync buffer output is fed to a digital multiplexer where either the buffer field sync or the TV field sync is transferred to the output.

There are four line sync receivers in the line sync channel which are all identical to the field sync receiver. The buffered TTL line sync signals are multiplexed with the TV line sync, under control of an instruction word, to form the line sync needed by the input processor function. The line sync like the field sync must be fast enough to reliably gate 40 MHz signals.

The built in test circuits are required to monitor the line and field sync outputs to check for their presence. This is done with two status flip flops which are cleared with a controller command, allowed to be set by a pulse occurring on the sync lines, and then read by the controller over a BIT status bus.

Analog to Digital Converter - The analog to digital converter digitizes the analog sensor video so that the sensor's image may be stored in the system's digital memory for display refresh. A single positive analog input with a full scale value of between 0.8 volt and 5.0 volts will be fed to the A to D function.

An input band limiting filter with a bandwidth which is adjustable between 1 MHz and 20 MHz eliminates those analog frequency components above 1/2 the sampling rate to prevent aliasing (the transformation of high frequency signals into false low frequency signals). The filter frequency may be set at 1, 2, 5, 10, and 20 MHz as determined by a controller instruction word.

A sample and hold circuit operating at the strobe rate feeds the sampled video to the conversion circuits which quantize the video into 16 levels. The sample and hold and converter circuits use high speed emitter coupled logic to allow conversion rates of between 2 MHz and 40 MHz. One of the two TTL conversion strobes from the standard or a special clock generator function are selected to drive the sampler and converter under control of a system instruction word. The converter outputs are translated to a 4 bit binary coded TTL output for transmission to the peak detection and memory functions. The converters quantizing level may be adjusted between 50 millivolts and 310 millivolts to provide the 0.8 volt to 5.0 volt full scale input. The Q level adjustment is under control of a system instruction word through a slow 6 bit digital to analog converter. It provides the only video gain or scale factor in the scan conversion functions. A manual video gain control is usually provided, however, on the display panel.

A built in test circuit consisting of a 4 bit line driver and address decoder sample the digitized video output upon command from the system controller and put the video code on the BIT data bus.

The complete A/D converter and video and sync receiver module has 35 inputs, 8 outputs, uses +5 volts, +15 volts, -15 volts, -5.2 volts, and consumes 8.9 watts. It contains 15 analog circuits, 10 digital small scale integrated circuits, 22 medium scale integrated circuits, and 167 discrete components.

2.6.2 Input Processing Logic Module

Module Requirements

This module accepts the digitized radar video data from the A/D Converter module and integrates the video over a number of sweeps determined by the Sensor Data Controller (SDC). The SDC also determines the bit length of the sweep and the integration constant. The radar video data is then peak detected to match the display format in range and truncated to the storage available in main memory. The peak detection rate and the truncation mapping is determined by the SDC. The integration provides an increase in the signal to noise ratio, and the peak detection and truncated logic are necessary to maintain the signal to noise ratio when the data is formatted for storage in memory. Built in test is required to determine if the module is functioning properly. A block diagram of this module is shown in Figure 9.

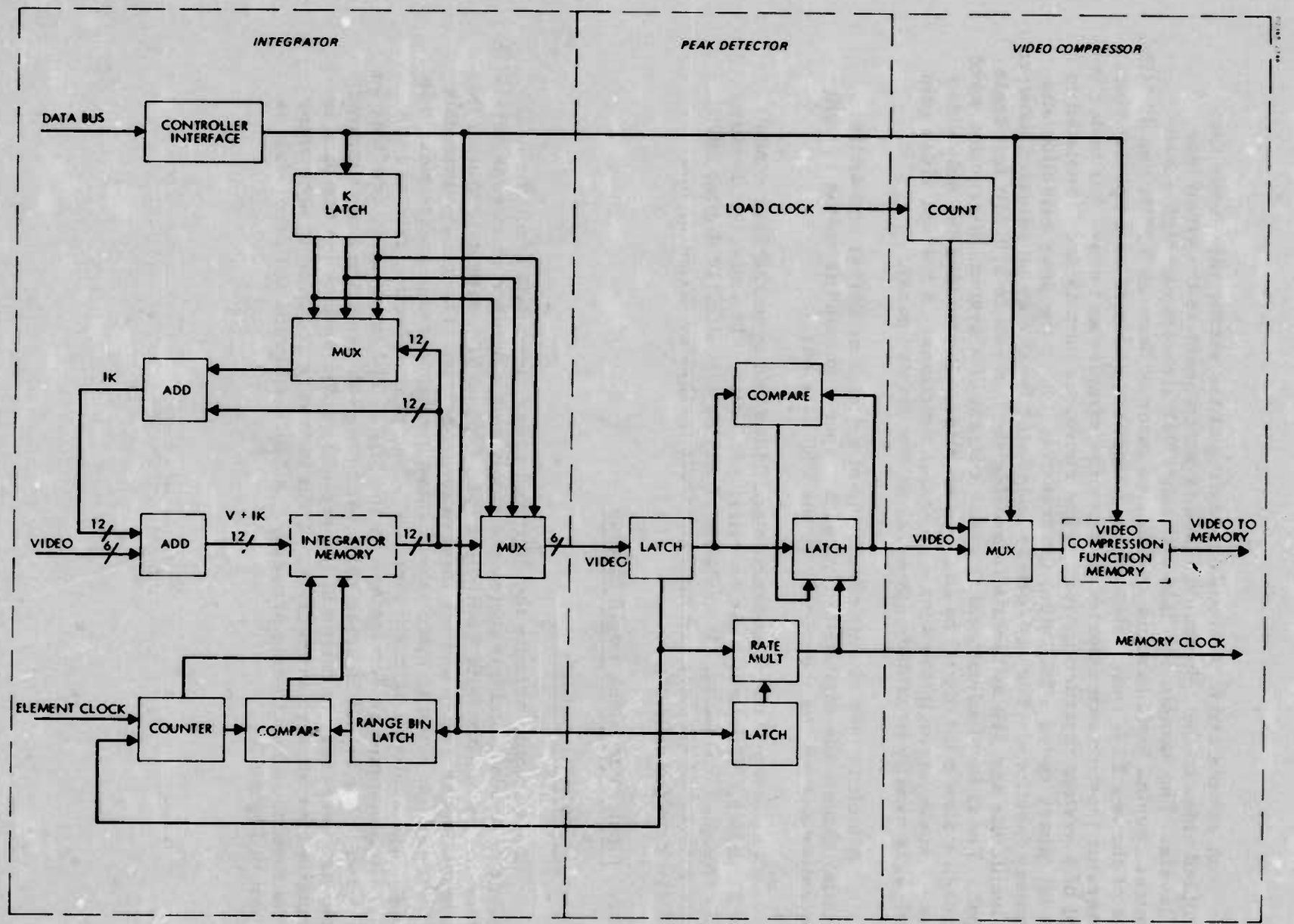


Figure 9. Input integrator, peak detection, and truncation logic module.

Signal	Number of Lines	Signal Type	Characteristics
Input Interface			
Sensor Video and clk	5	4 bit parallel data	10 MHz word rate
		1 TTL CLK	2048 bits per sweep
Data Bus	10	10 bit parallel data word, TRI state data bus.	1 MHz word rate
Address Bus	9		
Sensor Line Sync	1	TTL Sync	4.1 KHz
Clock Enables	5	TTL Logic	4.1 KHz
Truncation Load Clk	1	TTL CLK	1 MHz
Memory Lines	55		
Output Interface			
Output Video and Clk	5	4 bit parallel data	10 MHz
		1 TTL CLK	1024 bits per sweep
Sync Threshold	1	Analog	DC Level (MSI only)

Module Description

Input Integrator - The input integrator is capable of integrating up to 12 bits of video at 5 different integrating constants and can operate to at least 10 MHz input data rate. The equation implemented is $I = KI_{old} + Video$ where K is of the form $2^m - 1/2^n$ for n = 1 to 5. The integration is capable of storing 2048 data points of each sweep.

Peak Detector - The peak detector truncates the data points of each sweep into the number stored in memory for the desired format. The peak or maximum value of the truncated points is transferred to memory to replace the storage of all points. The peak detection is only done on 10 of the 12 bits at 10 MHz.

Video Truncation - After peak detection has been performed, the 10 bits of video is truncated to the number of bits available for storage, usually 3 to 6 bits depending on the type of video. This truncation must also operate at 10 MHz. The truncation mapping can be updated in 100 μs since some systems require dynamic truncation.

Mode Storage - Data latches and decoders are provided to hold mode data from the Sensor Data Controller. Memory and memory loading circuits are also required for the truncation mapping.

Clock Gating - Clock gating is implemented to provide the proper timing for each phase of all functions.

2.6.3 Integrator and Truncator Memory Module

Module Description

The Integrator and Truncator Memory Module is required to store 2048 twelve-bit words of radar video for integrating the incoming video and 4096 five-bit words for tuncating the integrated video. This module interfaces directly with the Input Processor Logic Module. A block diagram of this module is shown in Figure 10.

Built in test on this module is performed by controller variation of the feedback constant while the output is being monitored.

Input/Output Interface	Number of Lines	Signal Type	Speed
Radar Video in	12	TTL	4 KHz
Radar Video out	12	TTL	1 MHz
Integrator address	11	TTL	1 MHz
Read/write	1	TTL	1 MHz
Truncator Video in	12	TTL	1 MHz
Counts, R/W	2	TTL	1 MHz
Truncated Video out	5	TTL	1 MHz

2.6.4 Controller Logic Module

Module Requirements

The controller must perform arithmetic and logic functions for control of the digital scan converter and symbol generator. It must accept interface data over a special 16 bit interface data bus, decode these data and send appropriate control words to the other modules to establish the correct machine

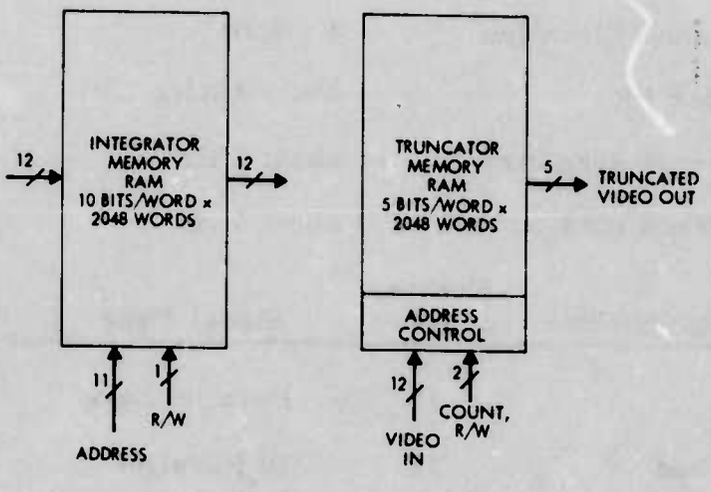


Figure 10. Integrator and truncator memory module.

state. It must be programmable to have sufficient flexibility to control the numerous existing systems and accomodate future systems. The controller must have at least a 16-bit wide word to generate accurate memory addresses or address slopes. The controller logic module block diagram is shown in Figure 11.

The inputs to the controller are:

+5, ground

Clock - 20 MHz

Mode word - 16 bits - pilot command rate - digital

Sensor Data

Antenna Azimuth	250 - 4 KHz (PRF rate)	- digital
Antenna Elevation	1 - 4 Hz	- digital
Radar PRF	250 - 4 KHz	- digital
Antenna scan direction	about 1 Hz	- digital
Antenna turn-around	about 1 Hz	- digital

Input/Output Interface	Number of Lines	Signal Type	Characteristics
Data Bus	16	Parallel data	4 MHz
Address Bus	11	10 Parallel + clk	20 MHz
Microprogram Control Word	32	Parallel data	4 MHz
Strobe Enables	7	Parallel data	20 MHz
Program address	12	Parallel data	4 MHz
Constant address	9	Parallel Data	4 MHz
Return address	12	Parallel Data	4 MHz
Primary Clock	1	TTL Clock	20 MHz
DAIS Control	2	T/R, Load	1 MHz

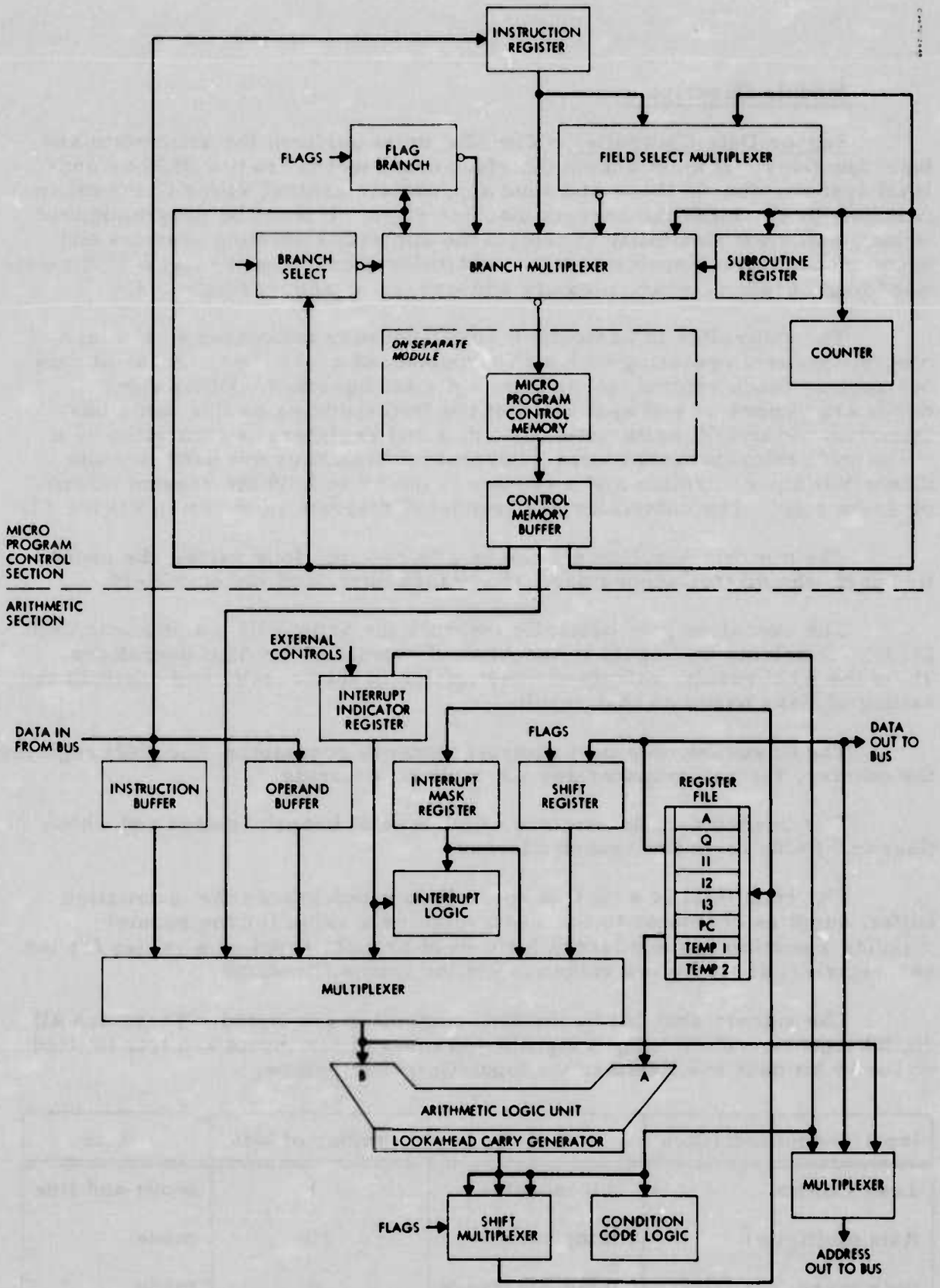


Figure 11. Controller module.

Module Descripton

Sensor Data Controller – The SDC must perform the arithmetic and logic functions. It must accept interface mode words from a DAIS or non-DAIS system, decode these and send appropriate control words to the other functions to establish the correct machine state. It must be programmable to have sufficient flexibility to control the numerous existing systems and accommodate future systems. The controller must have at least a 16 bit wide word to generate accurate memory addressess or addressing rates.

The controller is basically a single address processor with micro-program control operating with a 250 nanosecond cycle time. A 16-bit data bus accepts mode control words from a digital interface. Other control words are generated and sent to all of the DSC modules on this same bus. Operation of the DSC arithmetic logic unit and registers is controlled by a 94-bit wide microprogram word. Several multiplexers are used to route data within the controller and a counter is useful to hold the present micro-program step. The controller register level diagram is shown in Figure 11.

The microinstruction set can be grouped into four parts: the execution part, the miscellaneous part, the branch part, and the emit field.

The execution part basically controls the sensor data arithmetic unit (ALU). It selects the inputs to the ALU, determines the ALU operations, shifts the ALU result, selects the destination of that result, and controls the setting of flags based on that result.

The miscellaneous part controls memory operations, the shift register, the counter, the sub-register and other minor controls.

The branch part determines which type of branch is used and which flags and fields form the branch address.

The emit field is a multipurpose field which masks the instruction buffer; supplies constants to the ALU; supplies a value for the counter; supplies a portion of the address for a field branch; supplies a values for the sub-register; and supplies values to set the status flip-flops.

The signals sent out by the DSC controller are listed. These are all digital signals. These output signals and most of the inputs are transmitted on the 16 bit data bus listed in the Input/Output Interface.

Input/Output Interface	Sent to	Number of bits	Rate
Load Clocks	All modules	1	mode and line
Rate multiplier	Integrator	10	mode
Sync level	Input receivers	6	mode

Input/Output Interface	Sent to	Number of bits	Rate
Data Select	Input receivers	3	mode
Feedback constant	Integrator	3	mode
Total number of Range Bins	Integrator	10	mode
Counter Clock	Truncator	1	mode
Data bits	Truncator	5	mode
MUX	Truncator	1	mode
Clock Rate word	GP Clock Gen.	10	mode
Clock Rate word	GP Clock Gen.	10	mode
Clock Rate word	GP Clock Gen.	10	mode
Clock Rate word	GP Clock Gen.	10	mode
Clock Rate word	GP Clock Gen.	10	mode
Horizontal Resolution	Sync. Gen.	10 (could be less)	mode
Vertical Resolution	Sync. Gen.	10 (could be less)	mode
Horizontal Start Point	Output Add. Gen.	10	mode
Vertical Start Point	Output Add. Gen.	10	mode
Horizontal delay	Output Add. Gen.	10	line
Vertical delay	Output Add. Gen.	10	field
X-slope	Output Add. Gen.	16	PRF
Y-slope	Output Add. Gen.	16	PRF

2.6.5 Sensor Data Controller Memory and Symbol Generator Controller Memory Module

Module Requirements

The sensor data controller memory module must store the control microprogram steps and send these out to the controller to route the data flow

and cause the proper computations to be performed. This microprogram memory must have a relatively fast access time or much of the controller time will be spent waiting for a new instruction. About 500 to 1000 microprogram words of 32 bits or more in width are needed for the digital scan converter controller. The sensor data controller memory is shown in Figure 12.

The symbol generator controller memory module requires additional memory above that described for the sensor data controller. About 4K x 16 more ROM is needed and 4K x 16 RAM is also required to contain the display generating program, utility routines, and display lists. This module is shown in Figure 13. (These two memory modules become a single combined controller memory in the LSI version.)

Signal	Number of Bits	Characteristics
Output Interface		
Microprogram Word	32	4 MHz
Data Bus	16	4 MHz
Control Bits	3	20 MHz
Input Interface		
Microprogram Address Sensor Data	10	4 MHz
Microprogram Address Symbol Generator Data	10	4 MHz
Display Program Address	12	400 KHz
Display List Address	12	1 MHz
+ 5	--	23 watts
+12	--	1.6 watts

Module Description

Microprogram Memory — Upon receipt of a 10 bit address from the program counter the microprogram memory sends out 32 bit wide control word to establish operating conditions in the controller module.

Display Generating Program — Twelve bit addresses from the controller module cause output of program steps. Each program step moves the microprogram counter through single or multiple microsteps to finally generate data display words for the display list.

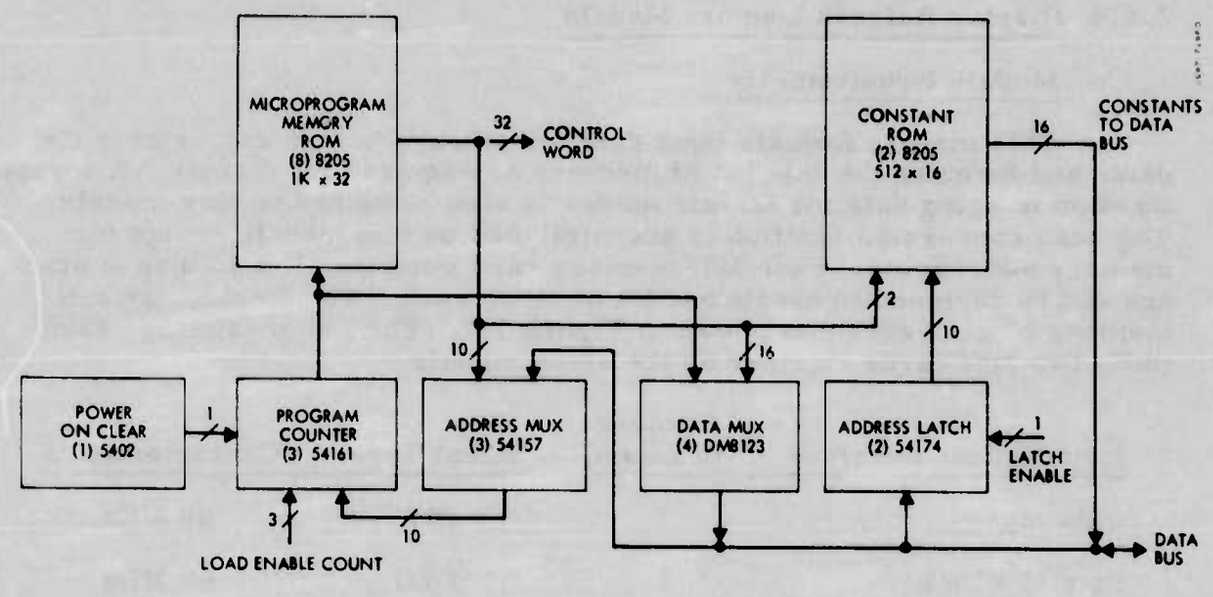


Figure 12. Sensor data controller memory.

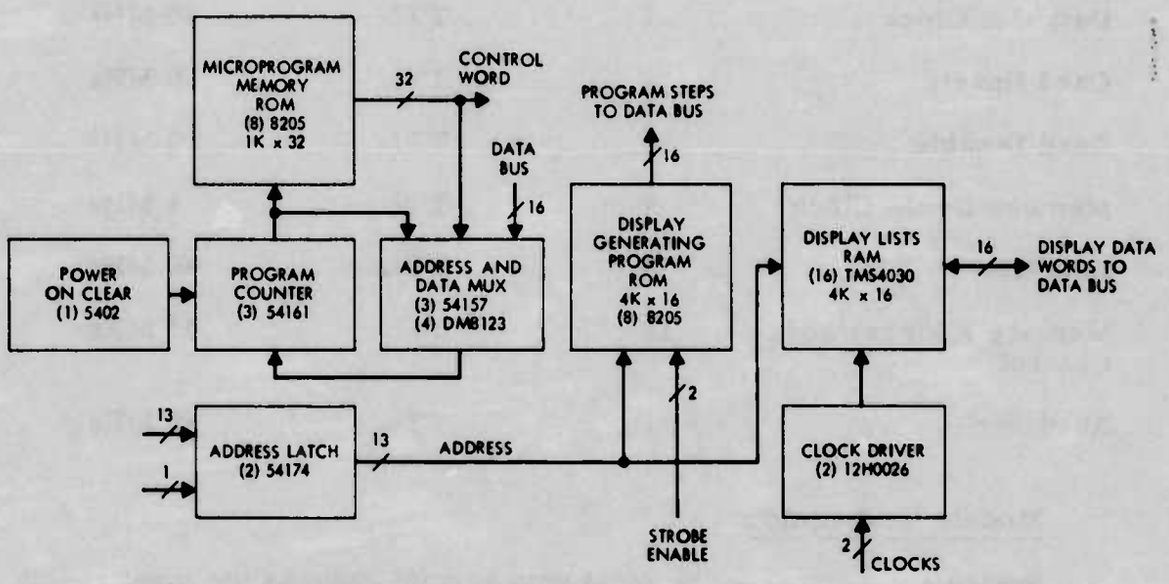


Figure 13. Symbol generator controller memory.

Display List RAM — The display list RAM accepts addresses from the controller and stores the controller generated data words in one section of the memory as the words are made available. In another section of the memory the complete previously generated display list is stored. Blocks or words of this complete display list are read out when requested by the symbol chain generator.

2.6.6 Display Refresh Memory Module

Module Requirements

This module formats input data for storage in memory, stores the data, and formats the data out of memory as required for display. A format function to aging data for air-air modes is also contained on this module. The scan conversion function is accomplished on this module except for memory addressing. Each MSI memory card contains 4K x 16 bits of storage and is designed to handle one bit of video each. The display refresh memory block diagram is shown in Figure 14. (The LSI version is essentially two MSI cards together on the same module.)

Input/Output Interface	Number of Lines	Signal Type	Characteristics
Data Input	1	TTL	40 MHz
Data In Clock	1	TTL	40 MHz
Data Output	1	TTL	40 MHz
Data Out Clock	1	TTL	40 MHz
Card Enable	1	TTL	10 MHz
Card Disable	1	TTL	10 MHz
Memory Cycle Clock	1	TTL	4 MHz
Data Out	1	TTL	40 MHz
Memory Address and Control	16	TTL	40 MHz
Read/Write	1	TTL	40 MHz

Module Description

Input Data Format — The input data format reduces the input speed of the data to the memory cycle speed. This is accomplished by serial to parallel transfer of the data. The data is then latched because of the data hold time of the buffer.

Input Data Buffer — The input data buffer allows asynchronous operation of the input data and memory. The FIFO buffer is required to allow sufficient time to load the memory. Since the maximum memory dimension is 512 elements, the FIFO must also be 512 elements long.

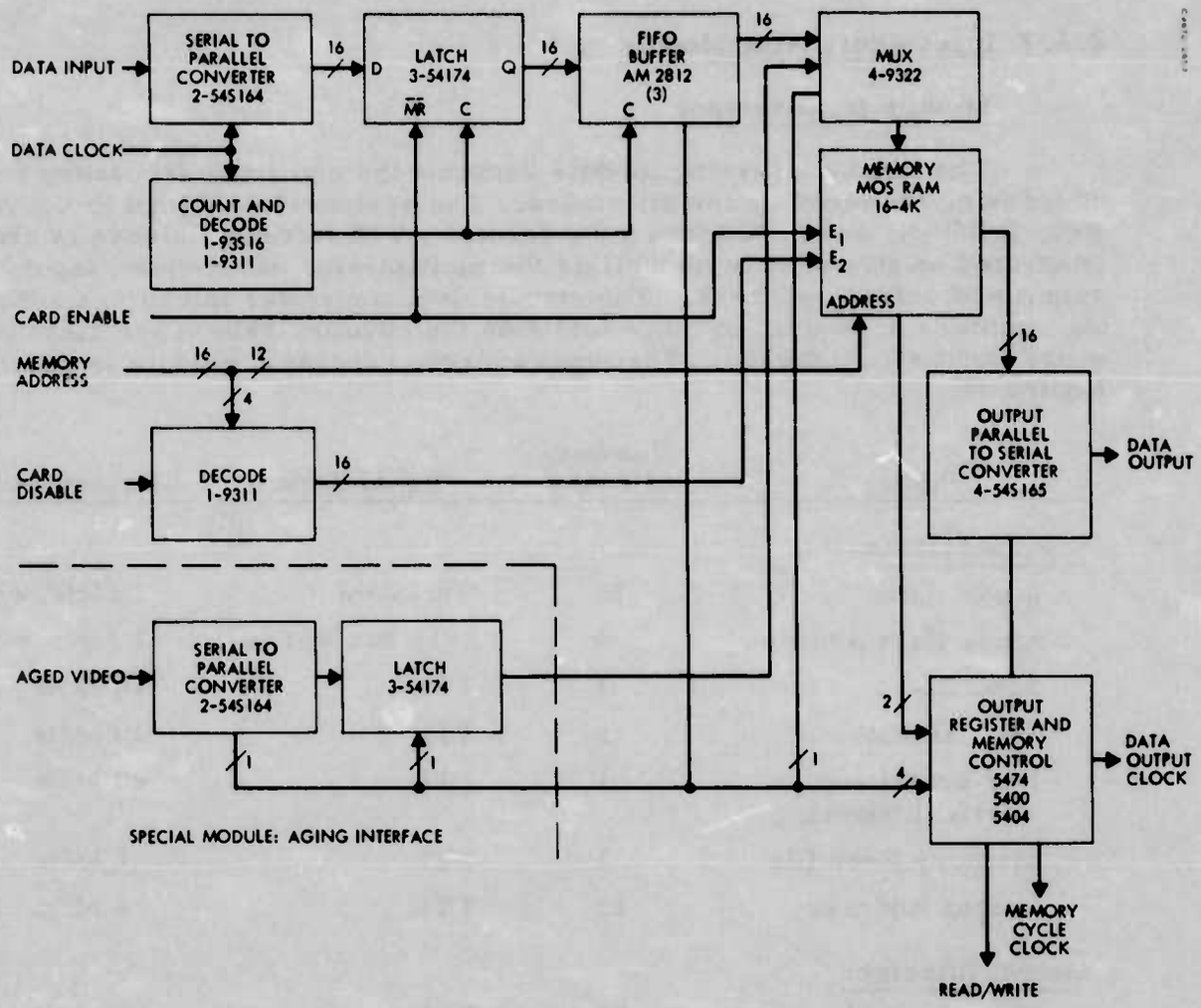


Figure 14. Display refresh memory.

Memory — The memory is composed of 16 - 4K MOS RAM's. The cycle time is approximately 400 NS.

Output Data Format — The output data format increases the data output speed to the TV necessary for display. This is accomplished by parallel to serial transfer of the data.

Voltage Aging Format — The Video Aging format circuit receives aged data and formats it to be loaded into memory. This function is required for most aging of air-air data. This circuit operates with an optional aging function module.

Built In Test — Built in Test of this module is performed in the controller by sensing the output signals based on an input signal inserted at the input of the scan converter.

2.6.7 Input Addressing Module

Module Requirement

The input addressing module contains the circuitry necessary for addressing the memory for all modes. The system is designed to convert PPI, B SCAN, and A SCAN to a TV format. The refresh address is also generated on this module as well as the multiplexing between the input/output and refresh address. The sensor data controller initializes addressing counters depending on mode and sets the counting rate at the start of every input sweep period. The input address generator module is shown in Figure 15.

Signal	Number of Lines	Signal Type	Characteristics
Input Interface			
Mode Data	16	Tri-State	1 MHz/word
Mode Data Address	9	6-16 Bit Words	1 MHz/word
Line Clk	1	TTL	10 MHz
Element Clk	1	TTL	10 MHz
Horizontal and Vertical Blanking	1	TTL	40 MHz
Memory Read Clk	1	TTL	1 MHz
Output Address	15	TTL	2 MHz
Output Interface			
Memory Address	20	TTL	2 MHz

Module Description

Mode Latch — A mode latch receives six 16 bit words from the sensor data controller (SDC) to determine mode status of the addressing circuitry. The proper latch is decoded by addressing from the SDC and multiplexed where necessary.

Slope Multiplier — The slope multiplier controls the frequency of the element address clock with respect to the line address clock. In some modes, as in PPI, the line address clock and the element address clock may be identical.

Start Position and Count — This circuit presets the element address and generates the element address by clocking a counter.

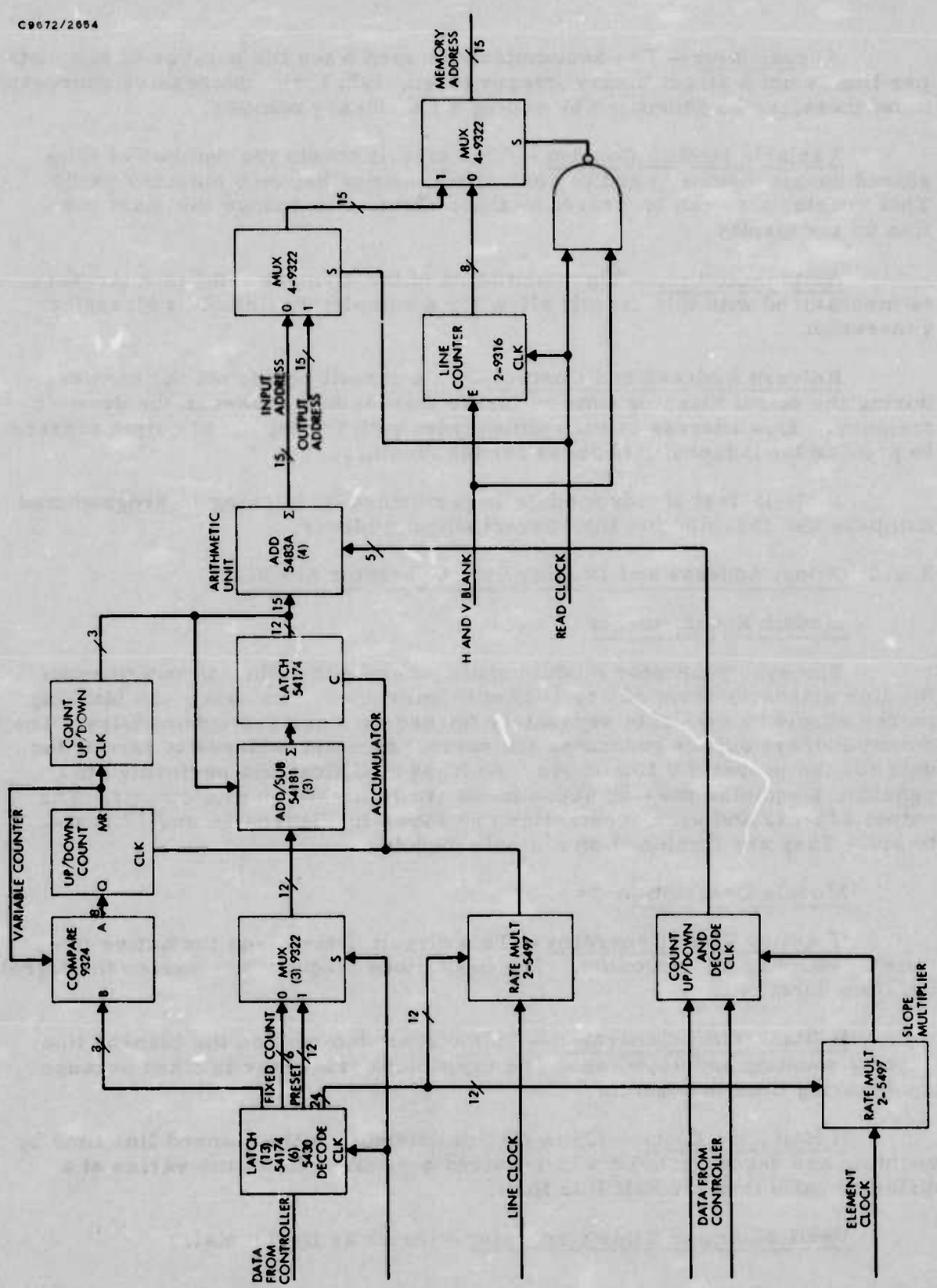


Figure 15. Input address generator module.

Accumulator— The accumulator is used when the number of elements per line is not a direct binary integer (e.g., 192,768). Successive addresses must therefore be generated by adding a non-binary number.

Variable Module Counter— This circuit counts the number of lines stored on one memory card to control addressing between memory cards. This counter also can be preset by the controller to change the start position on the display.

Arithmetic Unit — The summation of the element and line addresses is mechanized with this circuit allow for a completely flexible addressing generation.

Refresh Address and Control— This circuit refreshes the memory during the output blanking time to insure that no data is lost in the dynamic memory. This address is then multiplexed with the input and output address to provide the composite address for the memory.

Built-in-test of this module is performed by latching in programmed numbers and checking for the correct output address.

2.6.8 Output Address and Display Sync Generator Module

Module Requirements

The sync generator module shall generate the EIA composite syncs for line standards from 525 to 1023 with interlace. The syncs and blanking pulses should be available separately for use by other system modules. The output address circuit generates the correct memory address to format the data for the proper TV line mode. Address modifications performed to generate a squinted passing scene mode are available on this circuit. The output address and sync schematics are shown in Figures 16 and 17 respectively. They are combined on a single module.

Module Description

H Active Time Generator — This circuit determines the active line time by counting and decoding. The input clock frequency is varied to control the time duration.

H Blank Time Generator — This circuit determines the blanked line time by counting and decoding. The input clock frequency is fixed because the blanking time is constant.

H Half Line Clock— (This circuit determines the blanked line time by counting and decoding.) This is required because active time varies at a different ratio than the half line time.

Vertical Active Time Generator — (Same as Horizontal.)

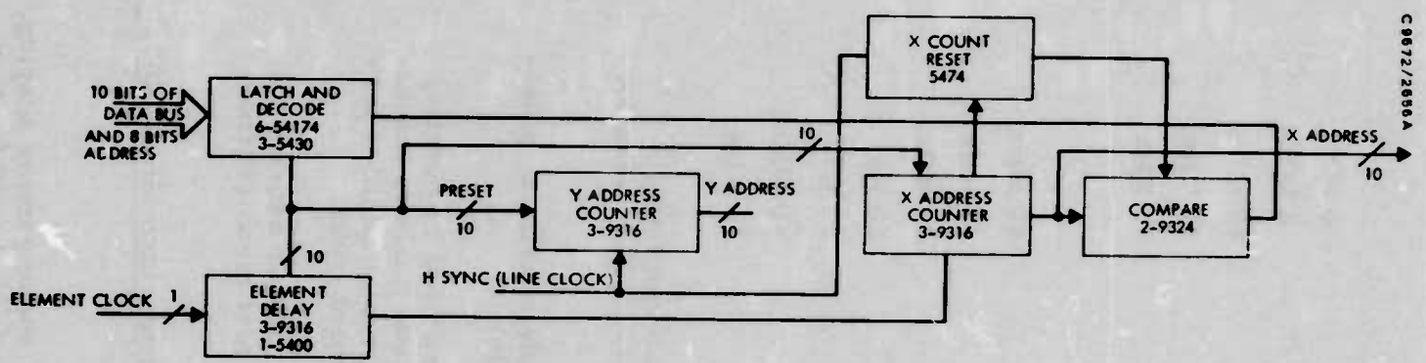


Figure 16. Output address generator.

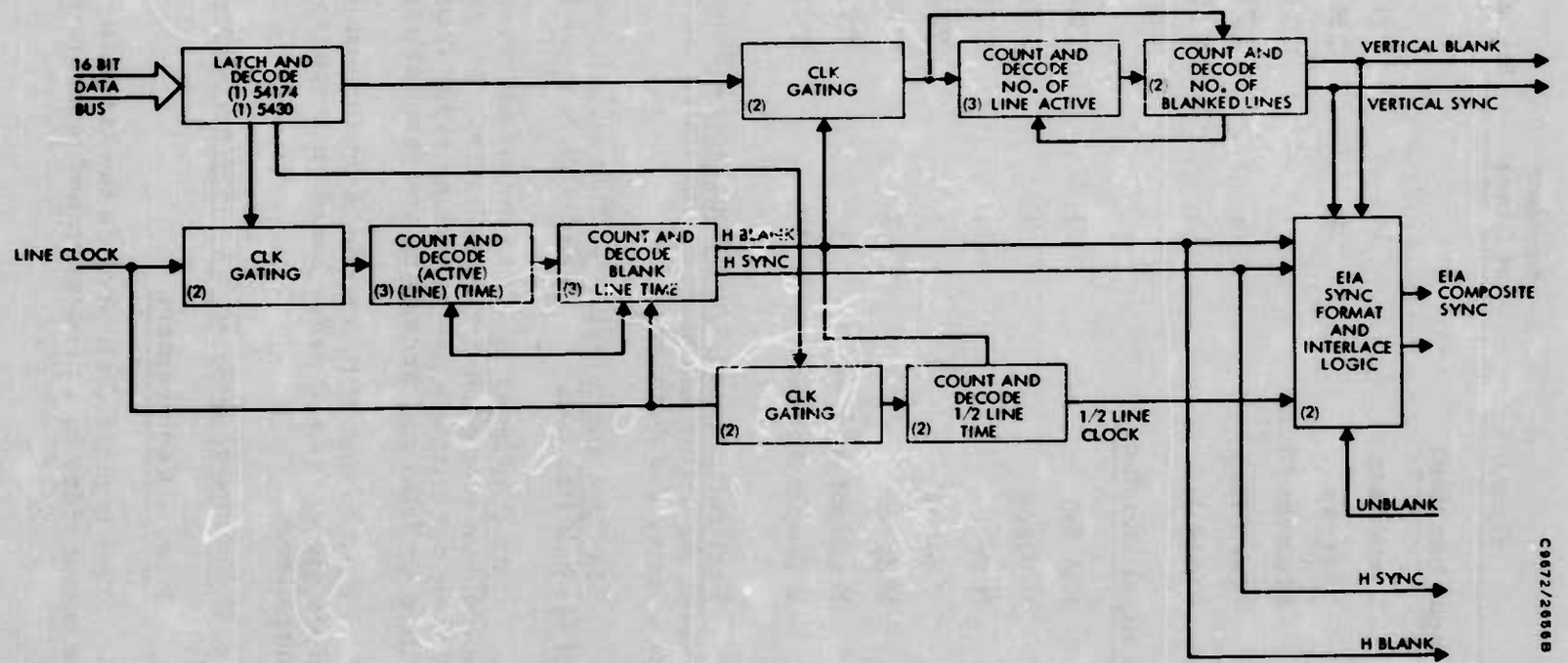


Figure 17. Sync generator.

Signal	Number of Lines	Signal Type	Characteristics
Input Interface			
Mode Data	10	Tri State	4 MHz
Address	8	Tri State	4 MHz
Element Clock	1	TTL	40 MHz
Line Clock	1	TTL	31 KHz
Unblank	1	TTL	31 KHz
Output Interface			
EIA Sync	1	TTL	40 MHz
H Blank	1	TTL	31 KHz
H Sync	1	TTL	31 KHz
V Blank	1	TTL	60 Hz
V Sync	1	TTL	30 Hz
X Output Address	10	TTL	40 MHz
Y Output Address	10	TTL	31 KHz

Vertical Blanked Time Generator — Since the same ratio exists between the active and blanked line time, the same input clock is used for this counter and decoder.

EIA Sync and Interlace — This circuit generates the equalizing pulses and the half line delay between fields to meet EIA standards.

Output Addressing — The output addressing is generated by counting the element clock and horizontal sync. The passing scene mode is mechanized by presetting a new start line every frame. The squint angle is formatted by delaying, presetting and terminating the element count.

Built in test of this mode is performed by the controller sensing the output addresses and syncs based on response to input test signal(s) from controller.

2.6.9 Gamma Shaper, D/A Converter, Output Filter and Video Mixer Module

Module Requirement

This module shall provide the capability for high speed gamma shaping, the output video in a predetermined manner requiring minimal modification.

The capability for converting the digital processed video to analog is contained on this module. The video output shall be filtered to minimize digitizing noise. (Frequency components beyond signal band limit.) Also summation of video with syncs, blanking, and symbology shall be provided on this module. All of these output processing functions are combined on the same module as shown in Figure 18.

Signal	Number of Lines	Signal Type	Characteristics
Input Interface			
VIDEO	6	TTL	40 MHz
VIDEO CLOCK	1	TTL	40 MHz
MODE DATA	6	Tri State	4 MHz
DATA ADDRESS	8	Tri State	4 MHz
COMPOSITE BLANK	1	TTL	31 kHz
COMPOSITE SYNC	1	TTL	62 kHz
SYMBOL VIDEO	1	TTL	40 MHz
SYMBOL BRIGHTNESS	1	Analog	DC Level
Output Interface			
COMPOSITE VIDEO	1	Analog	2 Vp-p 40 MHz

Module Description

Gamma Shaper — The gamma shaper receives 40 MHz video data from the memory with up to 6 bits of intensity resolution. To increase the number of visible gray shades on the display, the gamma shaper maps the 64 input intensity codes into another set of 64 output codes. The output has an 8 bit resolution which provides 256 possible brightness values from which to select.

The intensity code conversion is performed in a set of two identical bipolar read only memories. To extend the frequency range of the gamma shaper, two ROMs are used on an alternating basis. The input intensity code is used to address the 64 words of the ROM while the 8 bit word output contains the desired intensity code. Built in test circuits sample the output video and transmit the intensity code to the controller over the BIT data bus

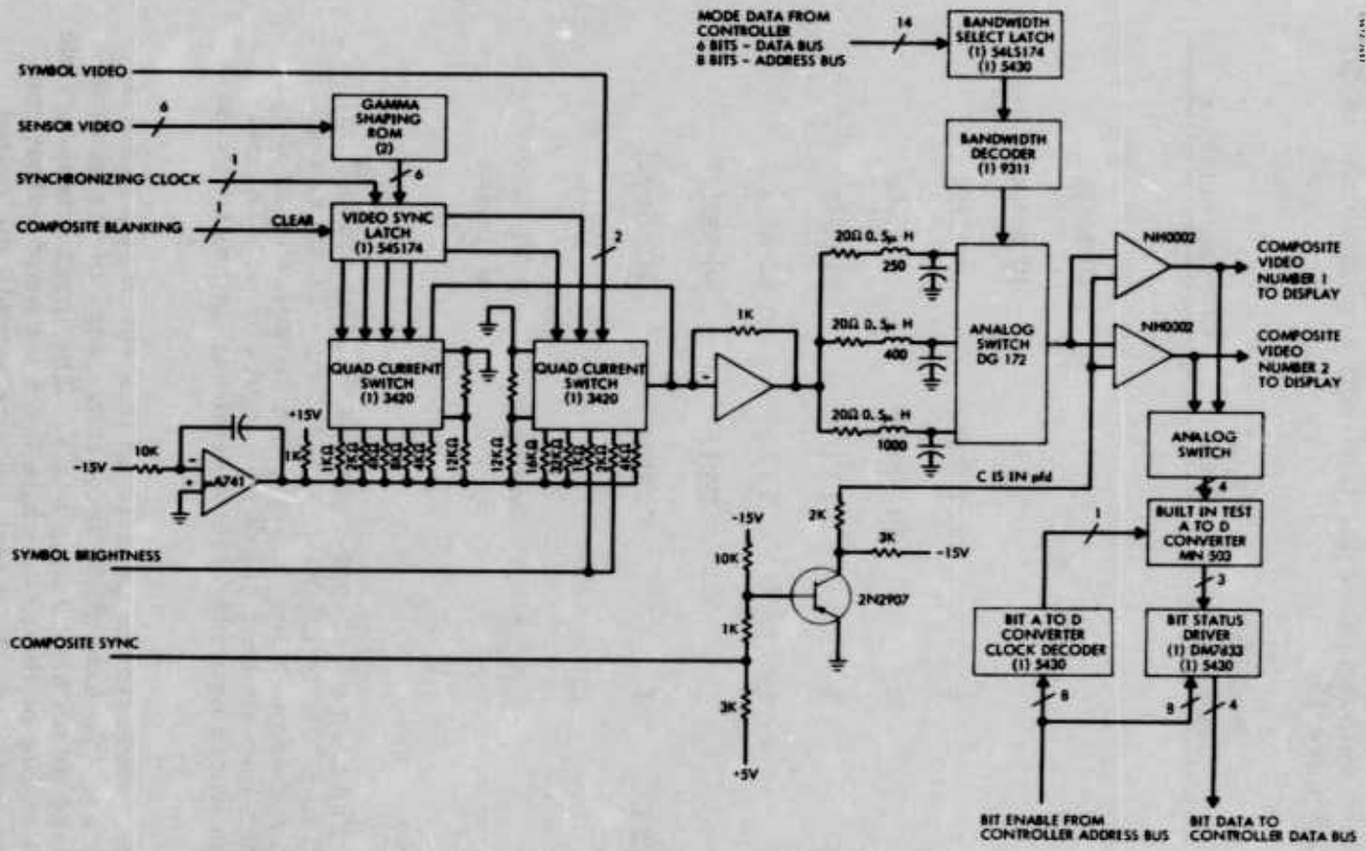


Figure 18. Video output D to A conv., video filter, and video mixer.

upon command of a special BIT test address input. The gamma shaper has 25 inputs, 14 outputs and consumes 1.8 watts of +5 volt power. It contains 4 small integrated circuits, 7 medium scale integrated circuits and 4 large scale integrated circuits.

Video Output Digital to Analog Converter - The D to A converter receives an 8 bit video intensity code at up to a 40 MHz rate. It also receives composite blanking to gate the video off during retrace. The circuit uses 8 current switches and a resistive ladder to reconstitute the analog video. A wide bandwidth current to voltage buffer amplifier transmits low output impedance video. The D to A has 15 inputs, one output, and consumes less than 1 watt total of +15 volts, -15 volts, and +5 volts. It contains an 8 bit high speed digital latch, 8 current switches, a resistive ladder and 2 operation amplifiers.

Output Video Filter - The video filter consists of three filter circuits each using a resistor, capacitor, and inductor. They have bandwidths of 2.5 MHz, 7.5 MHz, and 20 MHz. Wideband input and output buffer amplifiers are also required. One of the three filters is switched into the video channel under control of an instruction word. The filter has 15 inputs, one output, and consumes 0.8 watts total of +15 volts, -15 volts, and +5 volts. The function three analog switches, 3 RLC filters, 2 analog amplifiers, one small scale integrated circuit and 2 medium scale integrated circuits.

Output Video Mixer - The output video mixer combines the filtered sensor video with the symbol video and the composite TV syncs. An analog switch adds a DC voltage which is controlled by the symbol brightness potentiometer on the display's front panel. The analog switch is controlled by the single bit digital symbol video code from the symbol generator. A second analog switch adds in the composite TV sync under control of the sync input from the sync generator. A line driver is used to send the composite video to the display function.

Built in test circuits convert the analog output voltage to a 4 bit digital code and then send the digital value to the controller over the BIT data bus upon command of a special controller address input. The mixer has 14 inputs, 9 outputs, and consumes 1.5 watts total of +15 volts, -15 volts, and +5 volts. It contains 2 analog switches, an analog line driver, an operational amplifier, an A to D converter, 2 small scale integrated circuits and a medium scale integrated circuit.

2.6.10 General Purpose Clock Generator Module

Module Requirements

This module must receive mode control data from the Sensor Data Controller and correspondingly generate clock pulses and enable signals

which perform the timing and synchronizing functions throughout the entire MMSDS: The seven basic functions required on this module are:

1) A gated data bus receiver to buffer the mode control words.

2) A variable frequency oscillator to generate the clocks for the senior input processing functions.

3) Clock enable circuits to start and stop the input processing and synchronize the data flow through the input processor.

4) A variable frequency oscillator to generate the clock for the memory output multiplexing functions and display sync timing.

5) An adjustable frequency divider to form the actual clocks which control the memory loading and unloading.

6) A variable frequency oscillator to generate the fundamental clocks for the Sensor Data and Symbol Generator Controller.

7) A Built In Test feature to check the presence of all clocks.

Due to the several high frequency (40 MHz) oscillators and the overall number of components this function requires two modules for the MSI implementation. The LSI version can be accomplished on a single module. The block diagram of this function is shown in Figure 19.

Signal	Number of Lines	Signal Type	Characteristics
Input Interface			
Mode Data	16	16 bit parallel data word on Tri-State Data Bus.	4 MHz Max. word rate
Data Address	9	5 true plus 3 complement address bits plus strobe.	4 MHz Max. word rate.
Sensor Line Sync	1	TTL Sync	270 kHz Max. frequency

(Continued)

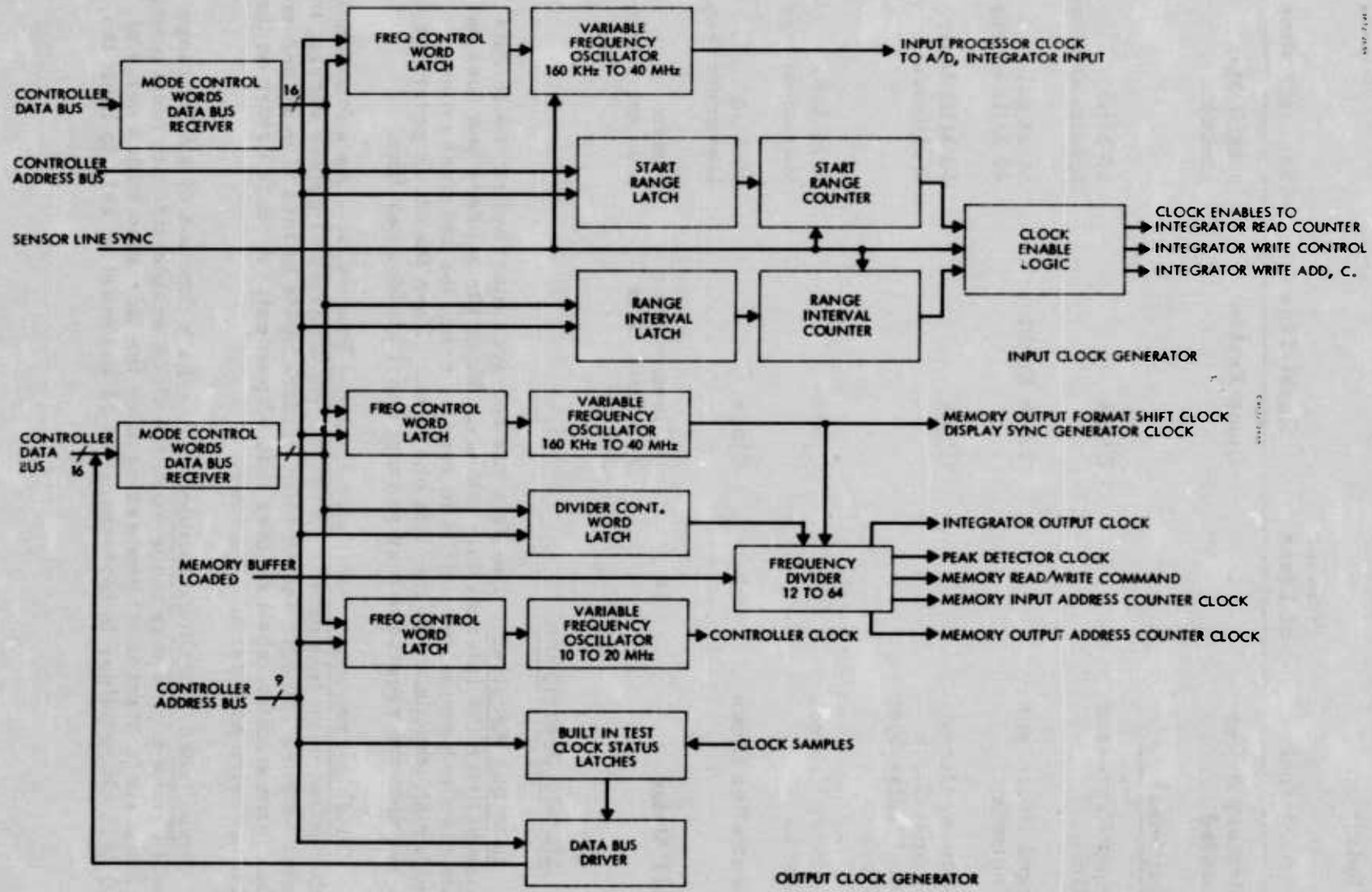


Figure 19. Modular multisensor display general purpose clock gen.

(Concluded)

Signal	Number of Lines	Signal Type	Characteristics
Memory Buffer Loaded	1	Clock Enable	1 MHz Max. frequency.
Output Interface			
Input Processor Clock	1	Clock	40 MHz Maximum Freq.
Input Processor Controls	4	Clock Enables	Must gate 40 MHz clocks
Memory Output Format Clock and Display Sync Clock	1	Clock	40 MHz Max. frequency
Memory Control Clocks	3	Clocks	1.28 MHz Maximum freq.
Controller Clock	1	Clock	20 MHz Maximum freq.
BIT Status	10	10 lines of the Tri-State Data Bus	4 MHz Maximum freq

Module Description

Data Bus Receiver - The data bus receiver must buffer the 16 data bus lines to drive the internal data latches. When the address bus does not indicate the clock generator unit is to receive data, the receivers must present a high impedance to the data bus lines. When the clock generator is to receive data the receivers may present one TTL load per line.

Variable Frequency Oscillator for Input Processor - As a function of a 12 bit control word this oscillator must form a series of pulses varying in frequency between 160 kHz and 40 MHz in increments of less than 10 percent. The long term stability shall be less than ±3 percent. A clock driver on the output must drive at least 30 TTL loads.

Input Processor Clock Enable Logic - As a function of a 6 bit range start word and a 6 bit range mode word the clock enable circuits must provide control signals to start input processing after the line sync with a delay of zero to 2016 clock pulses in increments of 32 and must be able to limit the

processing interval to a value between zero and 2016 clock pulses in increments of 32. The 4 output control signals are to be skewed by 1, 3, 4, and 5 clock pulse periods to compensate for delays within the input processor in order to align the data properly.

Variable Frequency Oscillator for Memory Control - As a function of a 12 bit control word this oscillator must form a series of pulses varying in frequency between 160 kHz and 40 MHz in increments of less than 10 percent. The long term stability shall be less than ±3 percent. A clock driver on the output must drive at least 30 TTL loads.

Frequency Divider - As a function of a 12 bit control word this circuit must divide the memory control clock by a factor of between 12 and 64 in increments of 1. Additional switching circuits must use the FIFO ready signal to gate the memory write command, FIFO load clock, and memory input address clock. The memory write/read command sequence must be modified by the control word to be, always low in the read only mode, alternating between write and read in the majority of modes, and write, write, read in the data feedback modes.

Variable Frequency Oscillator for Controllers - As a function of a 6 bit control word the oscillator must form a series of pulses varying in frequency between 10 and 20 MHz in increments of less than 1 MHz. The long term stability shall be less than ±3 percent. A clock driver on the output must drive at least 20 TTL loads.

Built In Test - Upon command of a control address word, a bank of 10 BIT latches are cleared. The latches are then set to the true state whenever the output clock connected to the corresponding latch changes state. The status of the latches, reflecting the clock operation, are applied to the data bus line with a Tri-State driver during the presence of the BIT read control address word.

2.6.11 Symbol List Decoder Module

Module Requirement

This module must receive symbol generator data words from the symbol display list and decode the data to control subsequent operations in the symbol chain generator module. Words in the display list may have a 4-5 bit identification or they may contain only data elements. The Symbol List Decoder must determine this and establish gate levels to route the data accordingly. This module must provide temporary storage for the 16 bit input data word, the number of segments in a data sequence, the length of the segments, and the video pattern of a repeated sequence. This module must supply the chain generator control signals, the mode control signals, the symbol list memory address word, the video level, and the symbol chain data to other modules.

The MSI module cannot contain the complete function so parts are moved to the chain generators. The resulting symbol list decoder module is shown in Figure 20.

Item	Received From	Number of Bits	Rate
Input Interface			
Bus Data	Symbol Gen. Controller	16	1 MHz
Bus Address	Symbol Gen. Controller	7	1 MHz
Data Bus Words			
Segment Length	Symbol Gen. Controller	12	200 kHz
Number of Segments	Symbol Gen. Controller	12	200 kHz
Video Pattern	Symbol Gen. Controller	12	200 kHz
Segment Blanking	Symbol Gen. Controller	4	1 MHz
Data Word Identification	Symbol Gen. Controller	4-5	200 kHz - 1 MHz
Output Interface			
Chain Gen. Control Word		12	1 MHz
Mode Control Word		12	1 MHz
List Memory Address		11	1 MHz
Chain Data		23	1 MHz
Video		1	1 MHz

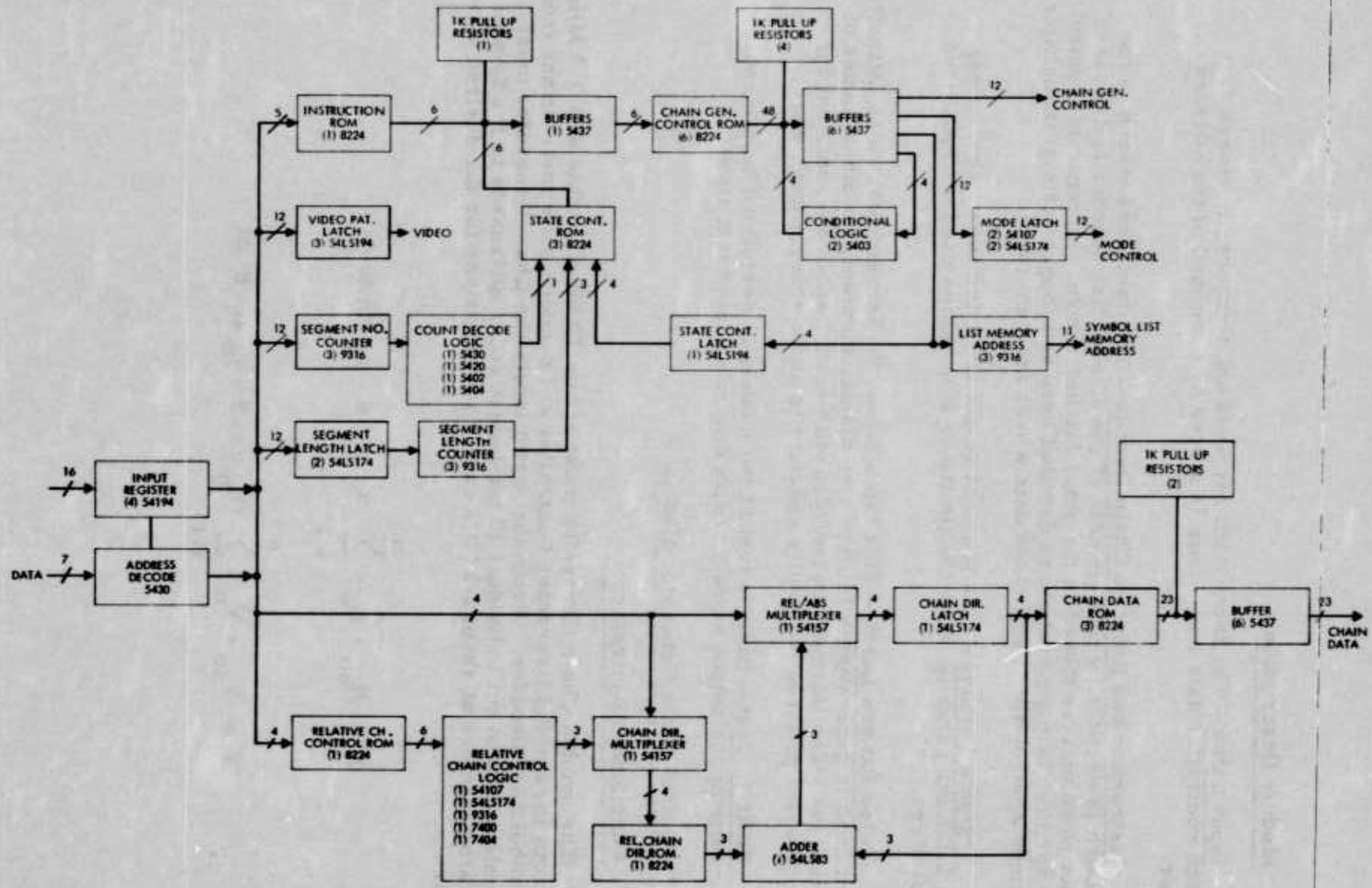


Figure 20. Symbol list decoder.

Module Description

Input Latch — The input latch receives and temporarily stores data from the controller data bus. Data is stored by command of the address decoder.

Instruction and Relative Chain Decode — The data word stored in the input latch is decoded by this element of the symbol list decoder and parts of the data word may be stored in the other latches shown. Incremental control words for the chain generator are decoded here and longer lasting or multiple step mode control words and chain data words are generated.

Segment Latches — The segment length latch and the number of segments latch temporarily store the limits or stop values used in repetitious control steps.

Video Pattern Latch — This latch stores the incremental video intensity pattern need in generating a limited size display element. In other modes of operation the video intensity is included with each display element, but for some repeated patterns it is more efficient to use a video pattern word.

Built In Test — Built in test of the module is performed by the controller sensing the output signals responding to an input test signal.

2.6.12 Symbol Chain Generator Module

Functional Requirements

The Symbol Chain Generator must accept 10 bit wide data at a 1-3 MHz rate from the Symbol Generator Controller and decoded state instructions from the Symbol List Decoder. From these two inputs the Chain Generator must assemble and send out individual 13 bit wide X and Y addresses to the Symbol Generator Memory at about a 1 MHz rate. The equations for the desired outputs are

$$X = H_{oo} + H_o + \sum_{i=1}^{n} (X_o \cos\theta - y_o \sin\theta)\,\Delta t$$

$$Y = V_{oo} + V_o + \sum_{i=1}^{n} (X_o \cos\theta + y_o \sin\theta)\,\Delta t$$

where

H_{oo} = horizontal bias

H_o = horizontal position

θ = rotation angle

X_o, y_o = 0, -1, +1

A single chain generator is shown in Figure 21. Two identical functions are required to provide the X and Y symbol generator function.

Input/output interface to the Symbol Chain Generator is listed below:

Item	Received From/Sent To	Number of Bits	Rate
Input Interface			
Symbol Data	Symbol Gen. Controller	16	1-3 MHz
10 Latch Enables	Symbol List Decoder	10	1-3 MHz
Clocks	Symbol List Decoder	1	1-3 MHz
X_o	Symbol List Decoder	1	1-3 MHz
Y_o	Symbol List Decoder	1	1-3 MHz
Output Interface*			
X_{out}	Symbol Gen. Memory	13	1 MHz
Y_{out}	Symbol Gen. Memory	13	1 MHz

*Data output by the Symbol Chain Generator is only X_o and Y_o.

Module Description

Six 10-bit wide latches temporarily store values of H_{oo}, H_o, cos θ, sin θ, V_{oo} and V_o. Sin θ and cos θ define a rotation and may remain unchanged for a complete template display list to depict a rotated scale. They are added or subtracted according to X_o, Y_o values to form the incremental terms in the equations. Those incremented terms are accumulated in the Fractional X and X accumulators. H_o and H_{oo} are added in and 13 bits of the resultant are sent out. The Y output is formed in an identical manner.

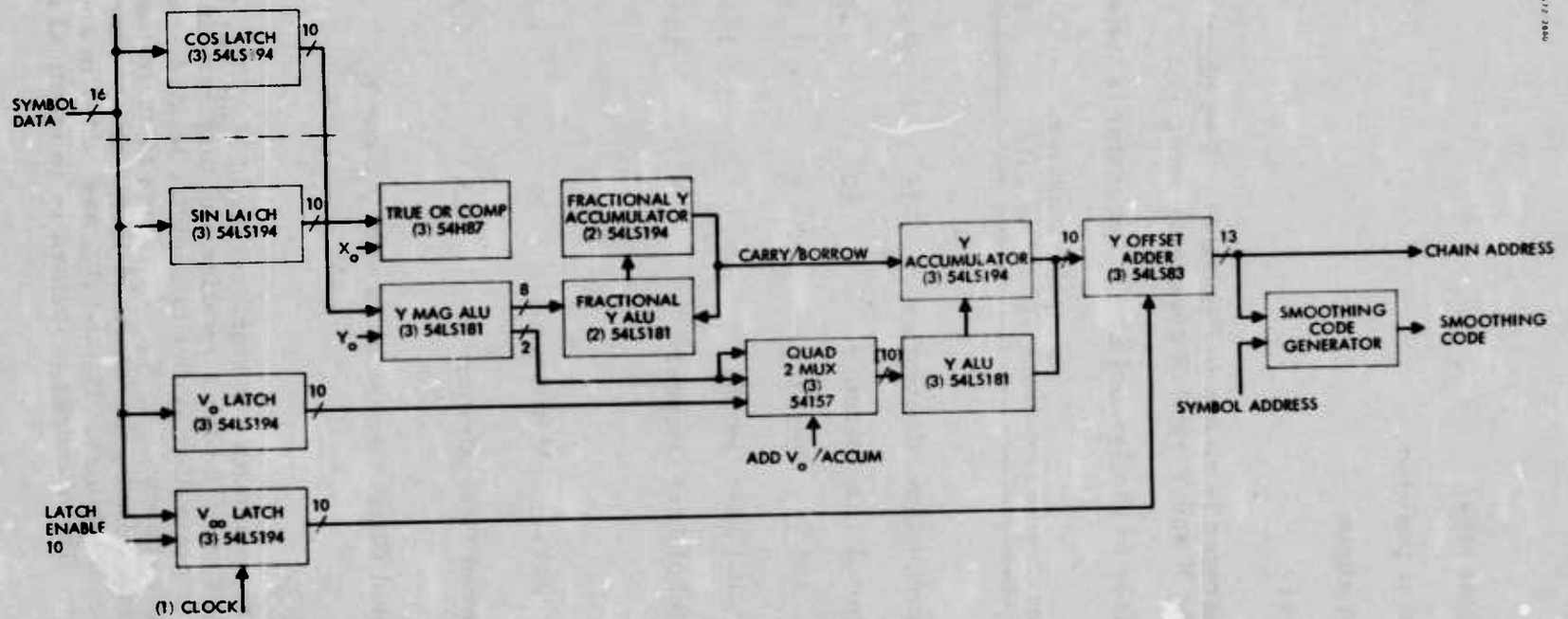


Figure 21. Symbol chain generator.

Built in Test – Built in test of this module is performed by the controller sensing the output X and Y signals in response to input test signals.

2.7 Special Modules

In addition to the core modules required in multiple applications, special modules are required for specific applications. These are modules that are not required in all applications. It is beyond the scope of this program to design all the special interface modules for all applications. However, in the applications analysis section, an estimate of the number of interface modules required for the various applications is presented. The specific system which is analyzed in that section does not possess any special interface modules since a DAIS interface is assumed.

Four special modules other than the interface modules have been identified. One is the nonlinear clock function to provide the terrain following and ground range sweep clocks. This is a special module because using present technology variable clock generation cannot be achieved accurately over a wide range (two or three orders of magnitude) without excessive complexity. The recommended mechanization employs a relatively simple design with a VCO. The same design can be used in multiple systems, but the VCO must be selected which operates over the range required. Therefore in effect, the VCO is the "special module" to be selected and used dependent on the specific application.

Another special module is the special video processing module. An attractive processing technique, histogram equalization was described in Section 3.0. It appears to have promise as applied to both radar and FLIR but further studies, lab evaluation and even flight test is recommended before incorporating such a technique as an actual module.

The third special module described is a unique module to perform display blanking outside the radar PPI sweep limits. The video ageing module is the last module discussed. Both this and the histogram module provide system growth potential functions. With further design effort it is possible that some or all of these special functions can be incorporated in core modules.

2.7.1 Non DAIS Interface Module

These modules are used to interface the Modular Multi-Sensor Display System with any system without a DAIS Interface. All signal inputs are formatted into a DAIS configuration to eliminate any modifications in core modules. All required analog to digital or synchro-to-digital conversion will be located on these modules.

Representative block diagrams for these modules are given in Figures 22 and 23.

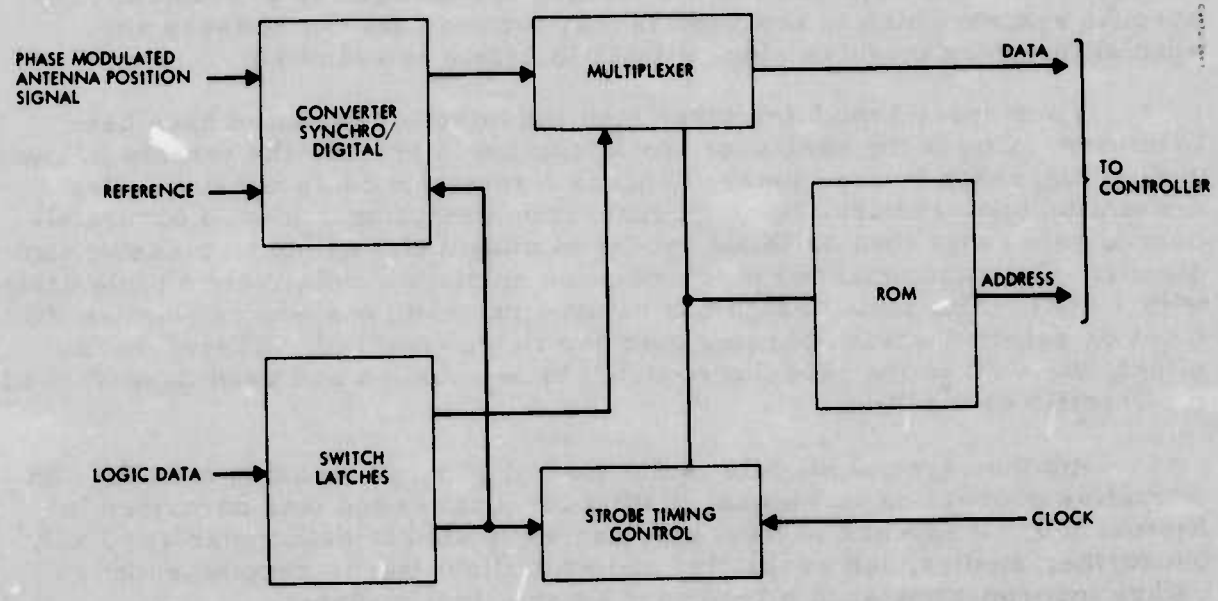


Figure 22. Non DAIS interface.

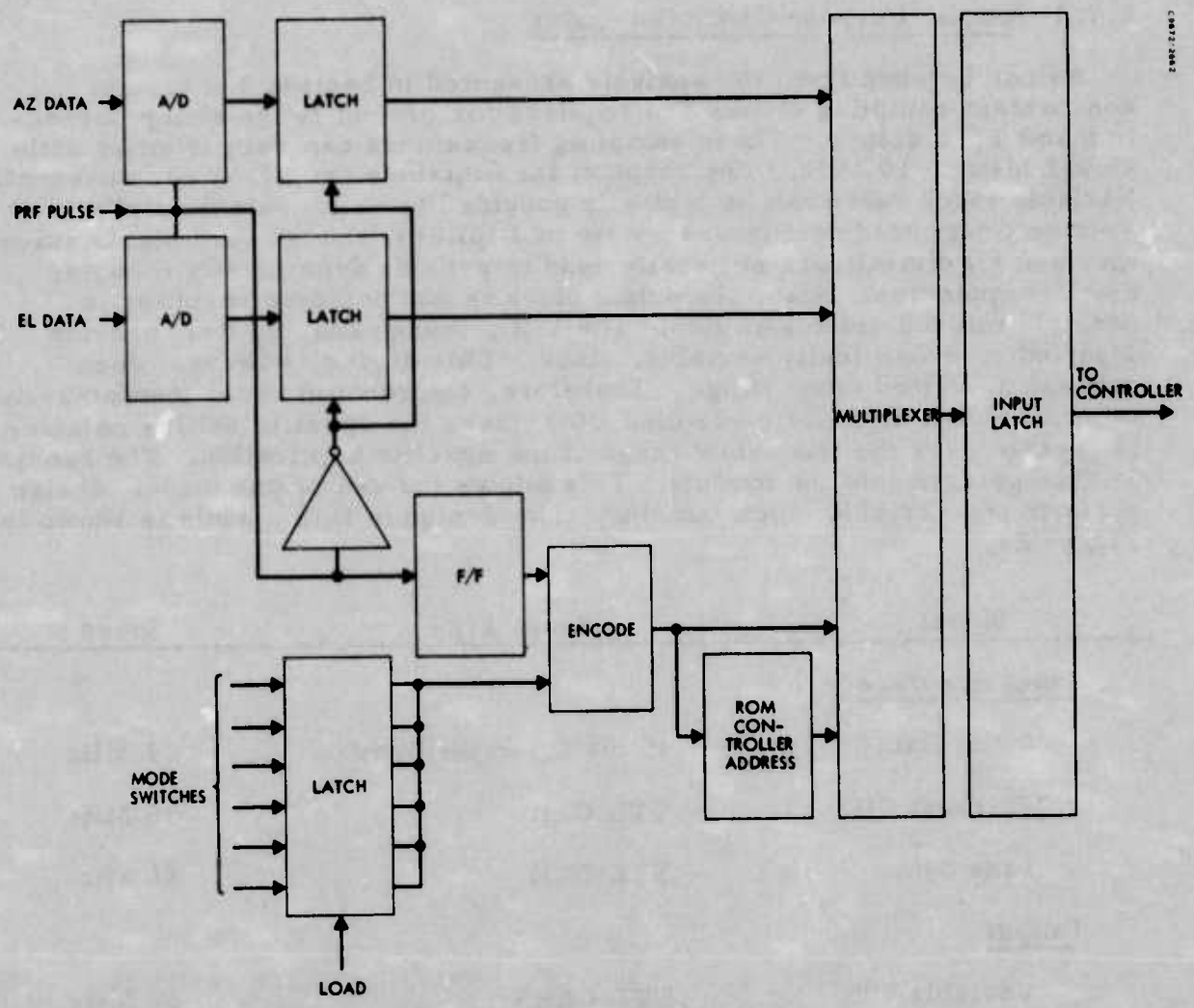


Figure 23. Non-DAIS analog interface.

Signal	Number of Lines	Signal Type	Speed
Output Interface			
Parallel data	16	Tri State T^2L	1 MHz
Input Interface	Depends on System Application (see Section 2.0)		

2.7.2 Special Purpose Clock Generator

As can be seen from the analysis presented in Section 3.0 special nonconstant sampling clocks are required for ground range sweep correction and TF displays. These sampling frequencies can vary from as little as 0.1 MHz to 10 MHz. The shape of the functions are also quite different. Variable clock rates can be typically provided by using rate multipliers or Voltage Controlled oscillators. Rate multipliers, though very stable since they are all digital, are not easily used to provide dynamically changing clock frequencies. Also, the output clock is non periodic resulting in possible missed video samples. The VCO, though analog, does provide a periodic, dynamically variable, clock. This device, however, does possess a limited clock range. Therefore, the recommended mechanization is to provide a digitally controlled VCO where the specific VCO is selected to operate over the frequency range of the specific application. The required VCO is plugged into the module. This allows the use of one module design to perform the variable clock function. The design of this module is shown in Figure 24.

Signal	Signal Type	Speed
Input Interface		
Mode Data	16 bit Tri State Word	1 MHz
Element Clk	TTL CLK	10 MHz
Line Sync	TTL CLK	40 kHz
Output		
Variable Clk	TTL CLKS	10 MHz

2.7.3 Radar Histogram Equalization Module

In Section 3.4 of Volume I, an attractive video processing technique, called histogram equalization, was discussed. A simulation was performed using simulated radar video. The results, though promising, did not warrant recommending that such a module be included. Further study analysis and the development of a BB of such a scheme is recommended before actual achieving an optimum module design. However, for the sake of completeness, a functional level design of one way of mechanizing such a technique in the modular system is shown in Figure 25.

The histogram equalization process as described in Section 3.4 (Volume I) is basically a means of truncating video whereby the resultant display possesses an equal number of picture elements at all intensity values. Therefore, the reasonable place to perform this function is at the point the integrator video is truncated for loading into the main memory. As presently mechanized, this truncation is achieved under control of the controller, but it

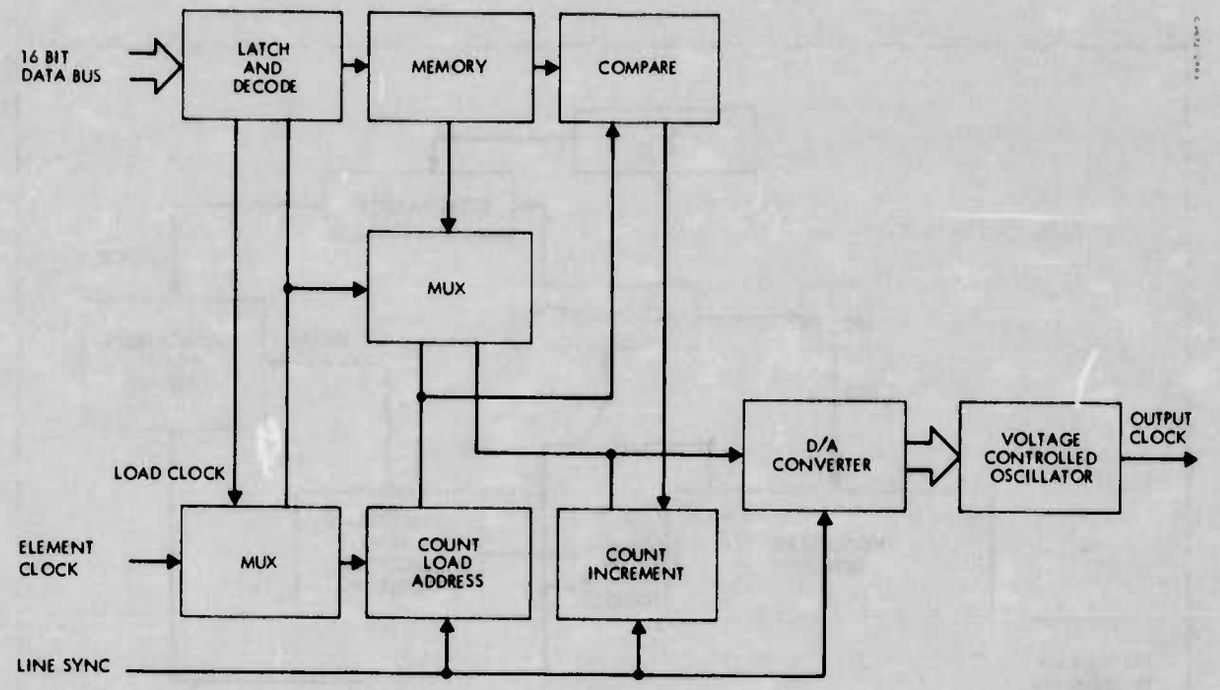


Figure 24. Special purpose clock generator.

is sufficiently flexible to allow control from a histogram processing module. Rather than receiving the truncation points from the controller, they are generated in the histogram processing modules and transferred to the truncator logic.

A block diagram of the histogram processing module is shown in Figure 25. While the integrator is read out, the actual video value is used to address a random access memory which originally is loaded with all zeros. The memory is organized such that there are as many addressable words as there are possible video intensity values carried in the integrator. Upon each addressing cycle, one is added to the stored word, thereby actually building up the histogram within the memory. Also during a complete integrator cycle, the video values are accumulated to a total sum (ΣT). Upon completion, the sum is divided by the number of values to which it is desired to truncate. (For example, if we store a 3 bit video, we must define 8 truncator points.) This division is achieved by shifting the proper number of bits forming $\Sigma T/N$. This represents the total number of picture elements to be stored at each intensity level. The final step then is to read out the histogram memory, in order, from an address equivalent to the lowest intensity value to the highest. The word values stored (histogram) are accumulated until the sum equals $\Sigma T/N$. At this point, the accumulator is reset and the histogram address is stored in a latch. When the memory is completely read out, the latched area represents the value of the truncation points (in a 3 bit system there would be 8 points). These truncation points are then used in the truncator logic to reduce the number of bits in the integrator to the number used in the main memory. It should be noted that it is not necessary to form the truncation points on every cycle of the integrator. In fact if the

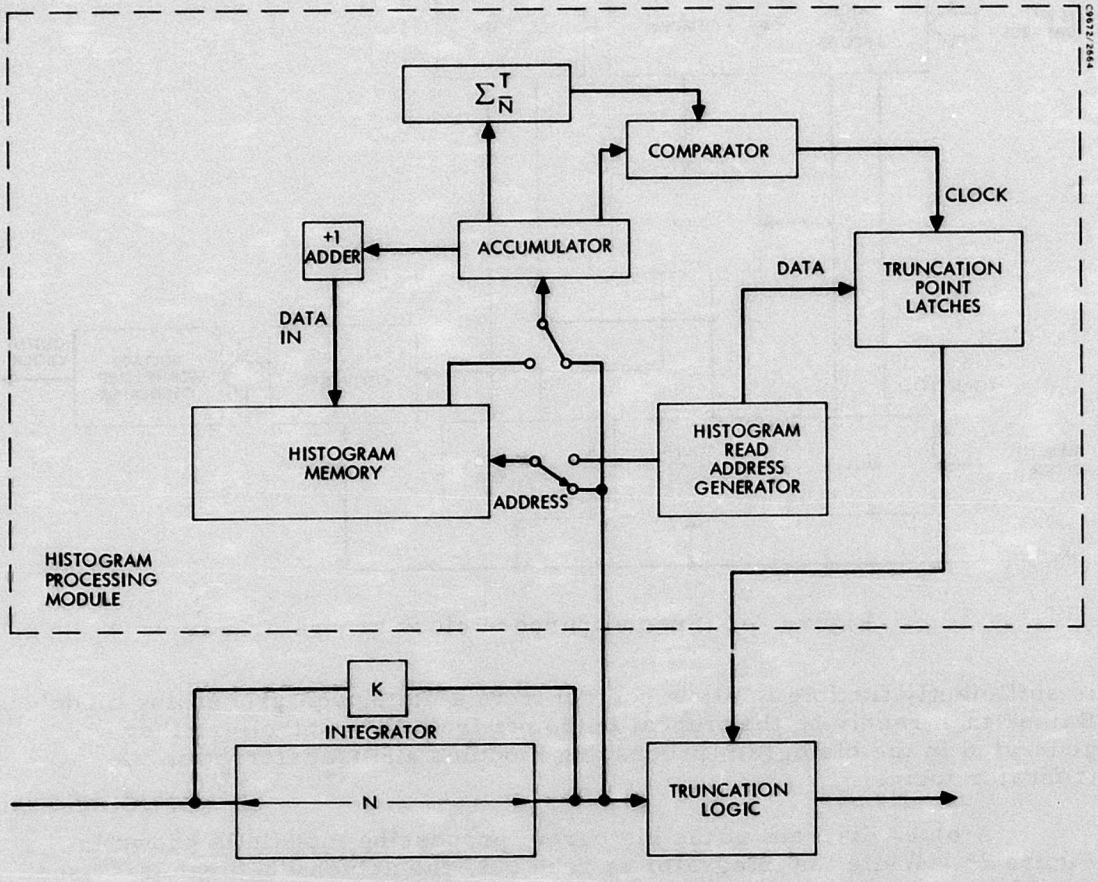


Figure 25. Radar histogram equalization module.

histogram memory is loaded in one cycle and several cycles are used to form the new truncation points, that should be acceptable. As mentioned earlier, in order to evaluate such a technique it is recommended that a breadboard be developed and integrated with an existing laboratory breadboard.

2.7.4 Out of Scan Blanking Module

The out of scan blanking module is a special module required in systems with a sector PPI format to blank the video at raster positions outside the scan sweep of the PPI. In the B-scan type formats this function is easily accomplished by the controller, but the complexity of the PPI mode necessitates a unique special module. The module design to perform the function is shown in Figure 26.

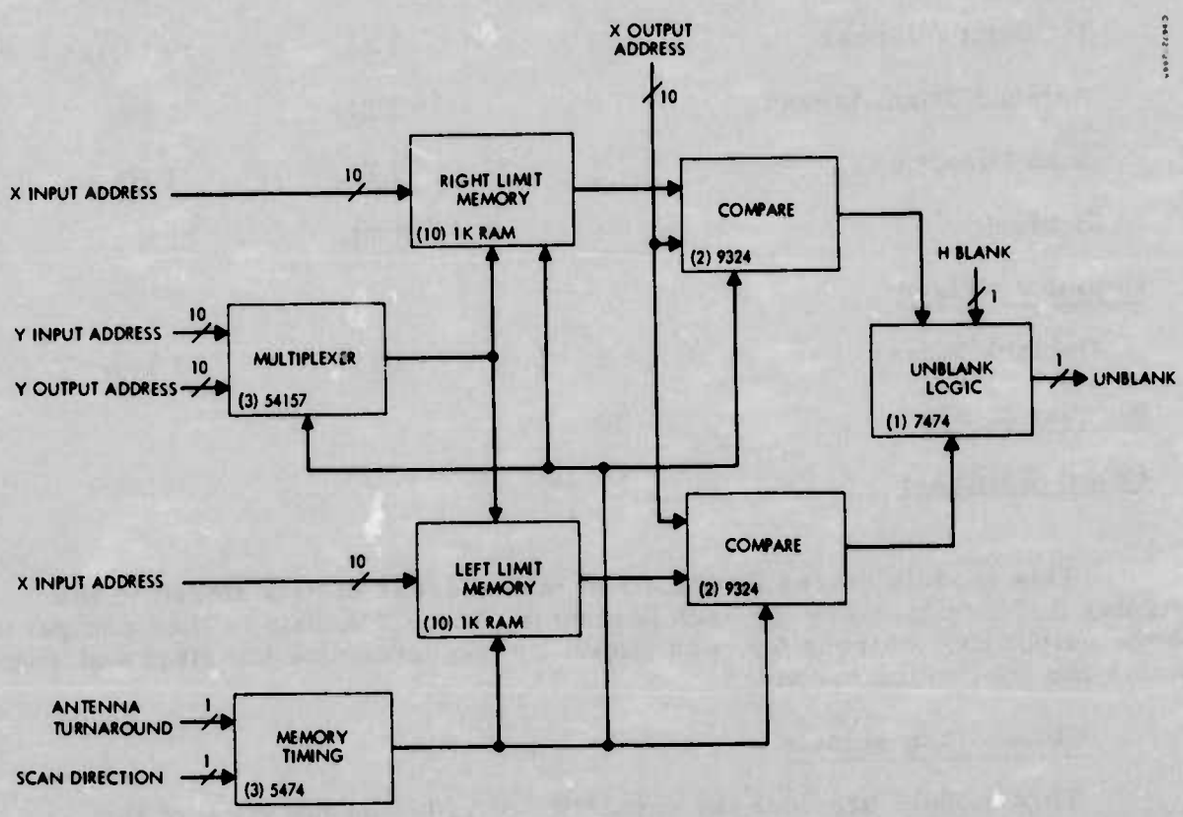


Figure 26. Out of scan blanking.

Signal	Number of Lines	Signal Type	Speed/Size
Input Interface			
X Input Address	10	TTL	10 MHz
X Output Address	10	TTL	10 MHz
Y Input Address	10	TTL	10 MHz
Y Output Address	10	TTL	10 MHz
Antenna Turn Around	1	TTL	1 Hz
Scan Direction	1	TTL	2 Hz
H Blank	1	TTL	31 kHz
Output Interface			
Unblank Signal	1	TTL	31 kHz
Number of ICs	30		
Power Estimate	17 W		

This module stores the first and last address of data stored in the Display Refresh Memory for each horizontal line. The data is then compared to the output line address for each output line to determine the start and stop points for unblanking the video.

2.7.5 Video Aging Module

This module provides the capability of reducing the value of the stored video under control of the system controller. Digital video is read out of the memory circulated through this module (Figure 27) decremented, and stored back into the main memory by way of the Aging interface (see Display Refresh Memory Description). This module can be used in two ways. If multiple intensity type is displayed, it essentially acts like a variable digital persistence module. If hit/miss video is stored, the new input video is stored with a maximum intensity value and by decrementing this value through this module a multi frame storage capability is provided.

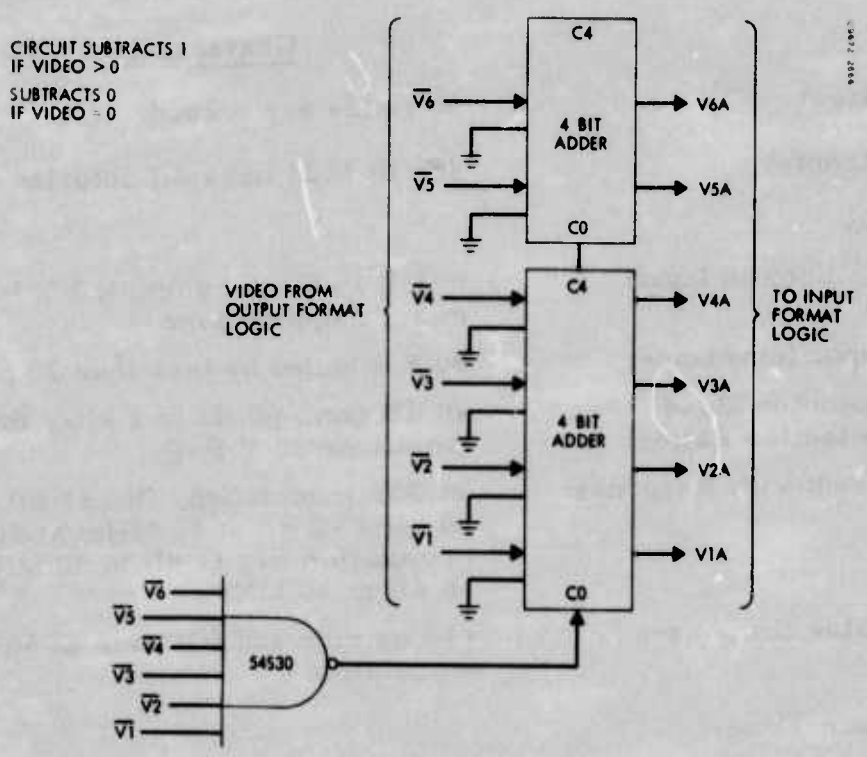


Figure 27. Video aging circuit.

2.8 Display Monitor Design

2.8.1 Functional Display Requirements

The Display monitor provides a high resolution TV display capable of operation over a range of horizontal line rates from 525 to 1023. The monitor can accommodate various size CRT's depending on the application. Standard modules are used to mechanize the monitor. These are:

- Horizontal AFC/Deflection
- Vertical Deflection/Sweep Fail
- Video Amplifier/Blanking
- Dynamic Focus/Horizontal Lingarity
- BIT Generator/Data MUX
- Low Voltage Regulators
- High Voltage Power Suppl·
- CRT

Typical performance characteristics for the monitor are:

	Characteristics
• Vertical	60 fields per second
• Horizontal	525 to 1023 lines 2:1 interlace
• Video	
Composite Input:	0.3 V P-P minimum; 3.0 V P-P maximum; negative sync
Input Impedance:	50 K shunted by less than 10 pF
Common Mode Rejection Ratio:	40 dB from 60 Hz to 1 kHz, maximum amplitude 20 V P-P
Frequency Response:	At 30% modulation, flat ±1 dB to 30 MHz -2 dB at 40 MHz; at 50% modulation flat ±1 dB to 30 MHz -6 dB at 40 MHz
Pulse Response:	<15 ns rise and fall time at 50% modulation
• Retrace Time	
Horizontal	5 μs maximum
Vertical	800 μs maximum
• Linearity	Horizontal and vertical linearity to better than 1% of display height, as measured on the horizontal and vertical center lines.
• Blanking	Vertical retrace and horizontal regenerated retrace blanking is provided
• High Voltage	15 KV to 20 KV adjustable encapsulated HV section <60 cubic inches ±0.1% regulation
• Dynamic Focus	Optimum focus is maintained at any deflection angle of the CRT electron beam

(Continued)

(Concluded)

Characteristics	
• CRT	
Size	6 to 12" diagonal
Brightness	>1000 FL
Spot Size	<10 MIL
Phosphor	P44
Light Filter	Matched bandpass
• Input Power	115 V 400 Hz ϕ A aircraft power 125 watts nominal

Signal	Number of Lines	Type	Characteristics
Input Interface			
115 V 400 Hz ϕA	1	Power	125 W
115 V 400 Hz ϕA RTN	1	Power	
Composite Video	1	Video/Coax	30 MHz
Bit Enable	1	Switched DC +12/GND	
Data Transfer Command	1	Pulse	
Output Interface			
BIT Data Word	8	8 bit parallel word	

Monitor Functional Description

The CRT monitor employs a wide range horizontal search and lock operation to permit use with any horizontal line rate from 525 to 1023. The wide bandwidth video amplifier ensures resolution while dynamic focus and a horizontal linearity correction scheme are used to provide a high quality TV raster display. A block diagram of the modular display unit is shown in Figure 28.

The vertical and horizontal deflection circuits are driven by the sync signals stripped from the composite input video. The horizontal is phase locked to the incoming rate by the horizontal AFC circuitry. The vertical

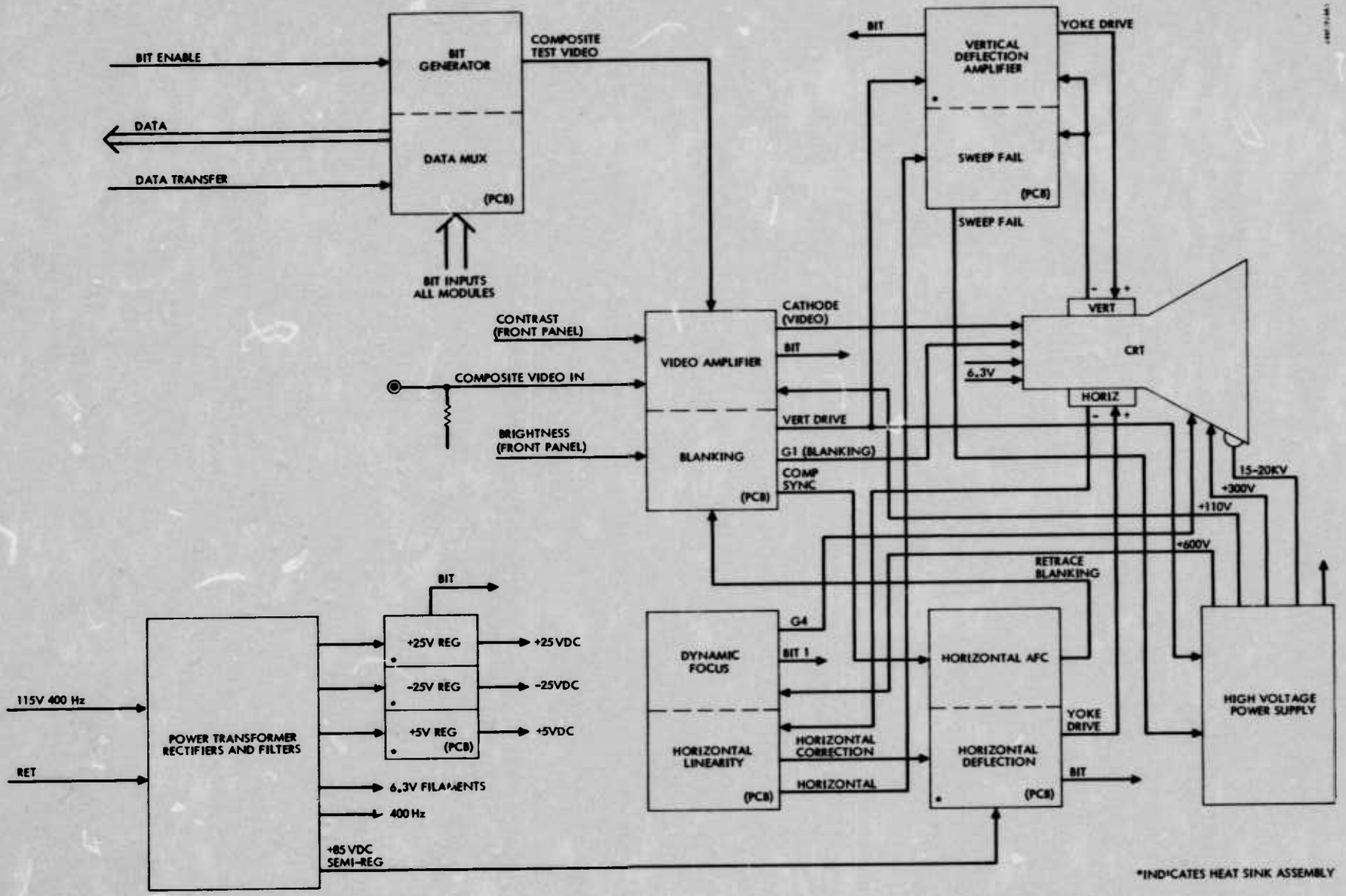


Figure 28. CRT monitor functional diagram.

deflection is provided by a linear amplifier while the horizontal deflection utilizes a low power reasonant tuned fly-back approach. A sweep fail circuit is used to disable the high voltage in the absence of a sweep.

The high voltage power supply is a DC-DC converter synced to the vertical field rate to prevent asynchronous noise from appearing on the display. All voltages required for CRT operation are generated in the high voltage power supply.

The monitor circuitry is capable of driving CRT's from 6 to 12 inches in diameter. The same modules are used regardless of the CRT size.

Built In Test capability is provided by the generation of an internal display pattern. A vertical 8 shades of grey pattern is generated upon receipt of the BIT enable signal allowing the operator to view the display and to make any front panel adjustments (i.e., contrast, brightness). During the time the test pattern is displayed each individual circuit module is monitored internally by the BIT circuitry and the results converted to a digital go-no go signal. This information is made available for transmission to the DSTU. By use of the internal BIT capability and viewing of the display during the test pattern fault isolation to a module can be accomplished in a minimum of time.

2.8.2 CRT Module

Functional Requirements

The CRT module will contain a magnetic deflected electrastatically focused CRT. All electrode potentials will be supplied by the standard high voltage module. The display unit can accommodate various size CRTs with from 6 inches to 12 inches diagonals. For the larger CRTs dynamic focus may be required to maintain spot quality.

Input Interface	Number of Lines	Signal Type	Characteristics
Anode Potential	1	15 KV - 20 KV	DC
Filament	2	6.3 V 400 Hz	0.6 A
G4	1	Dynamic Focus	Horizontal line rate

(Continued)

(Concluded)

Input Interface	Number of Lines	Signal Type	Characteristics
G2	1	300 VDC	DC
G1	1	Blanking	Composite horizontal and vertical
Cathode	1	Video	±1 dB to 30 MHz -2 dB @ 40 MHz with 30% modulation -6 dB @ 40 MHz with 50% modulation

Module Functional Description

The CRT module will consist of the CRT envelope, deflection coil, and electromagnetic shield potted around the CRT.

Light filters can be separately attached to the front of the CRT housing.

2.8.3 Video Amplifier/Blanking Module

Functional Requirements

The video amplifier and blanking module receives composite video from the DSTU and provides drive signals to the CRT module and horizontal and vertical sync pulses to other modules as shown in Figure 29.

The functional requirements of the module are to perform video preamplification, video drive, DC restoration, sync separation, and generate composite blanking for the CRT control grid.

Signal	Number of Lines	Signal Type	Characteristics
Input Interface			
Composite Video in	1	Video	30 MHz
Test Video	1	Video	4.5 MHz
Contrast	1	Front Panel Control	DC

(Continued)

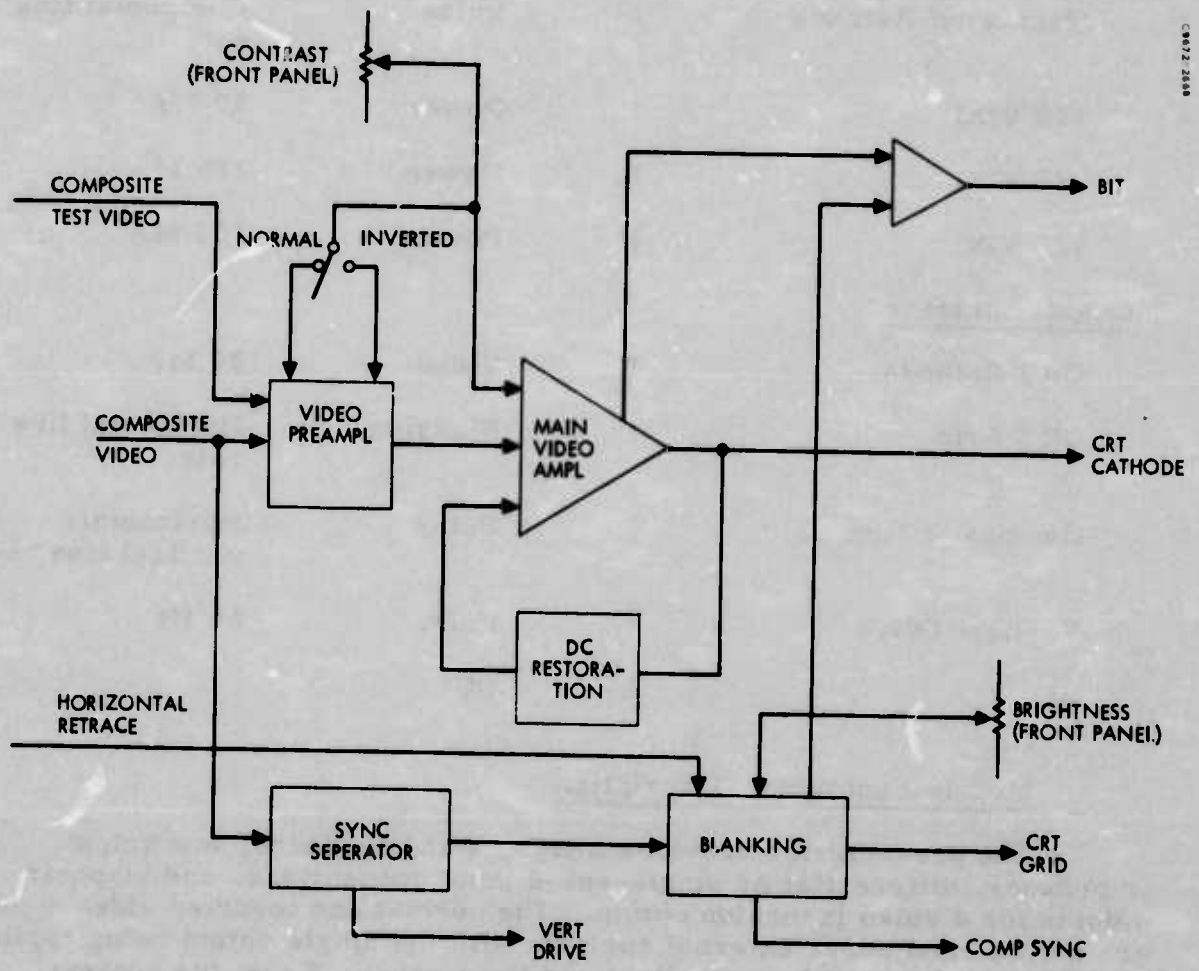


Figure 29. Video amplifier/blanking module.

(Concluded)

Signal	Number of Lines	Signal Type	Characteristics
Brightness	1	Front Panel Control	DC
Horizontal Retrace	1	Pulse	Horizontal line rate
110 VDC	1	Power	30 MA
+25 VDC	1	Power	150 MA
-25 VDC	1	Power	100 MA
Output Interface			
CRT Cathode	1	Video	30 MZ
CRT Grid	1	Blanking	Horizontal line rate
Composite Sync	1	Pulse	Horizontal/ vertical line rate
Vertical Drive	1	Pulse	60 Hz
BIT	1	DC	

Module Functional Description

The preamplifier provides a high input impedance, low output impedance, differential or single-ended input connections, and bi-polar outputs for a video inversion option. The normal and inverted video signals are multiplexed under external control, with the single output being applied to the contrast control on the display's front panel. From the contrast control the video is AC coupled to the main amplifier where the bias is held constant by DC restorer action. The main amplifier maintains its large signal gain out to 30 MHz with good stability assured through use of feedback around the entire circuit. The DC restorer samples the video output during each horizontal retrace interval, at the end of the horizontal sync pulse, and holds that level until the next retrace sample is taken. The video sample is fed back to the input of the main amplifier where it acts as an error signal to keep the output black level constant regardless of input amplitude or contrast control settings. After leaving the main amplifier, the video goes directly to the CRT cathode.

Since the horizontal and vertical sync signals are mixed in the input video, the display must strip them off the video in order to control the raster

sweeps. In conjunction with the DC restorer circuits the negative sync signals are clipped off the composite video at the black level. A sync separator operates on any degree of interlace or non-interlace and with or without equalizing pulses to provide the flexibility required to drive a wide variety of TV formats.

Regenerated retrace blanking is accomplished by combining inputs from the sync separator and horizontal retrace to form a composite blanking signal to drive the CRT control grid. The positive peaks of the blanking pulses are DC restored to the brightness control setting.

A test video is provided under the control of BIT which will provide a shades of grey test pattern in a standard 525 line format.

2.8.4 Horizontal AFC/Deflection Module

Functional Requirements

The horizontal AFC/deflection module provides the ability for the horizontal deflection system to operate between various line rates between 523 and 1023. Also contained on this module as shown in Figure 30 is the wide frequency, energy conserving deflection system. Functions performed on this module include:

- Horizontal line AFC
- No-sync detection
- Picture phase correction
- Yoke driver switching circuits
- Horizontal deflection power supply

Signal	Number of Lines	Signal Type	Characteristics
Input Interface			
Composite Sync	1	Pulse	Horiz. Line Rate
Horiz. Linearity Corr.	1	Ramp	Horiz. Line Rate
+85VDC	1	Semi-Regulated Power	.4A
+25VDC	1	Power	200 MA
-25VDC	1	Power	150 MA
+5VDC	1	Power	250 MA

(Continued)

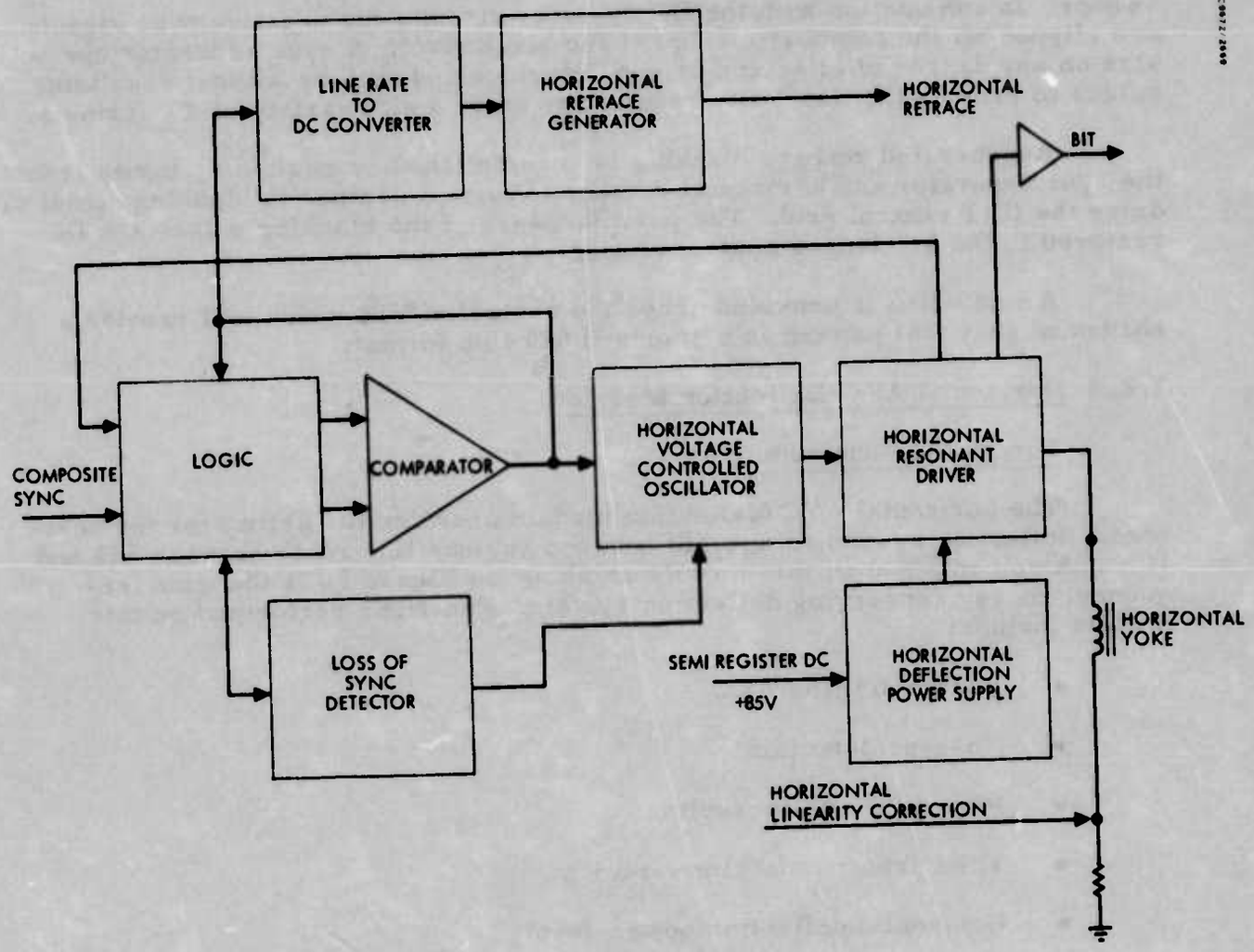


Figure 30. Horizontal AFC/driver.

(Concluded)

Signal	Number of Lines	Signal Type	Characteristics
Output Interface			
Horizontal Drive	1	Pulse	Horiz. Line Rate
Horizontal Retrace	1	Pulse	Horiz. Line Rate
BIT	1	Pulse	Horiz. Line Rate

Module Functional Description

The horizontal frequency control system will automatically track and lock onto any horizontal rate between 7.5 KHZ and 35 KHZ. A DC voltage for controlling the frequency of the horizontal oscillator is derived from an early-late pulse comparator system in which the horizontal oscillator rate is compared against the rate of incoming sync pulses.

To prevent tearing of the display during momentary loss of sync the error input is disconnected from the voltage controlled oscillator for several milliseconds allowing the VCO output to remain constant.

The line rate to voltage conversion controls the width of the horizontal retrace as a function of line rate to obtain correct display phasing with different line rate inputs.

The horizontal yoke driver uses an energy conservation technique where the yoke resonates with a capacitor to generate a half sine wave of about five microseconds under all line rate conditions. During the second half of the horizontal sweep, energy is taken from the deflection power supply and stored in the horizontal deflection yoke. After the resonant retrace, the current in the yoke has reversed and energy is delivered from the yoke back to the power supply.

Deflection energy for the horizontal yoke is provided by a line rate controlled power supply which provides a constant display width, independent of the incoming line rate.

A BIT output is provided to monitor the function of the module.

2.8.5 Vertical Deflection/Sweep Fail Module

Function Requirements

The vertical deflection/sweep fail module accepts the vertical sync pulse and generates the linear drive for the vertical deflection yoke. Sweep fail protection is also provided in the advent of a loss of sweeps. A schematic of this Function is shown in Figure 31.

Signal	Number of Lines	Signal Type	Characteristics
Input Interface			
Vertical Sync	1	Pulse	60 HZ
Horizontal Sweep	1	Ramp	Horiz. Line Rate
+25VDC	1	Power	.5A
-25VDC	1	Power	.5A

(Continued)

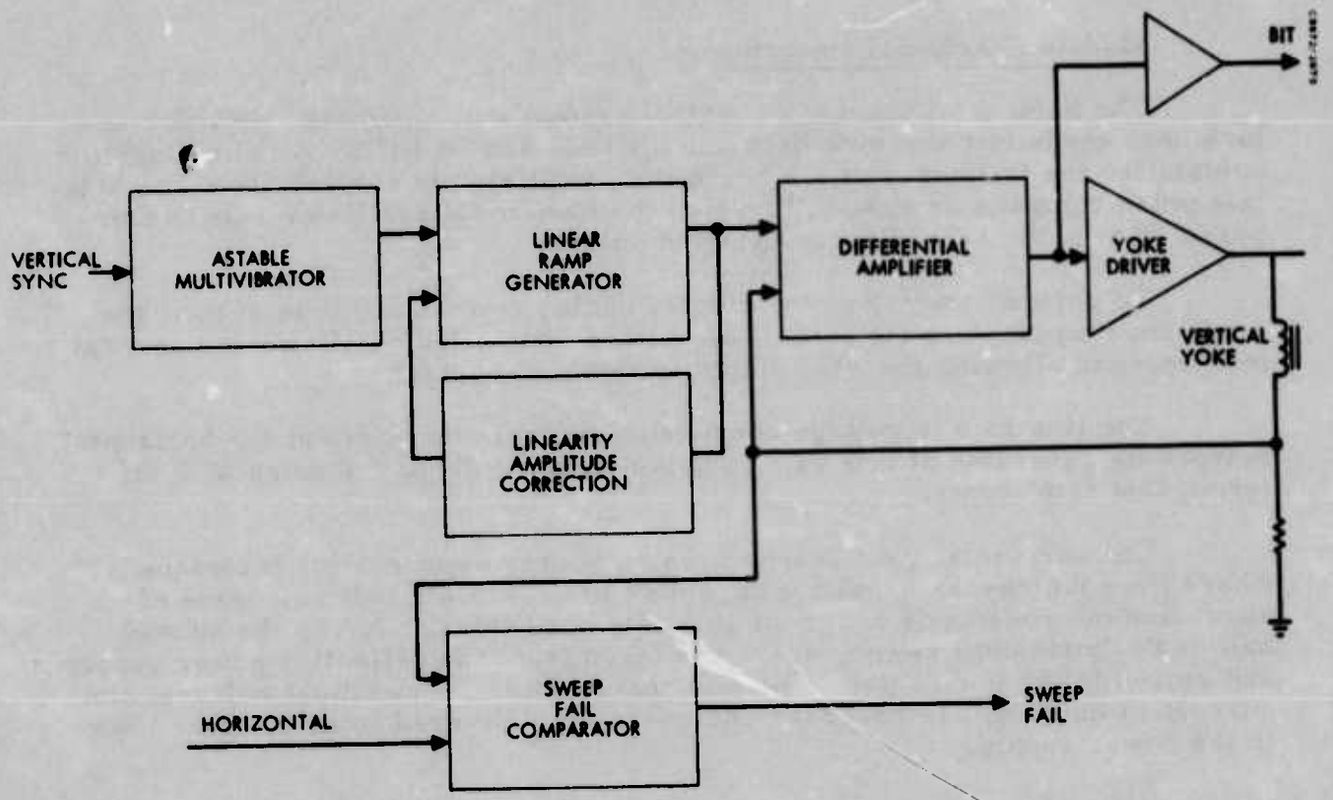


Figure 31. Vertical deflection/sweep fail.

(Concluded)

Signal	Number of Lines	Signal Type	Characteristics
Output Interface			
Vertical Drive	1	Ramp	60 HZ
Sweep Fail	1	Switched DC -25V/Open	
BIT	1	Ramp	60 HZ

Module Functional Description

The vertical sync pulse locks the astable multivibrator to the vertical field rate. The output of the multivibrator is used to drive a linear ramp generator which converts the pulses to a linear ramp which is used to drive one side of the differential amplifier. The other side is driven by an error voltage which is proportional to the current in the yoke. In this manner linearity is maintained throughout the amplifier.

Sweep fail protection is generated by DC conversion of the vertical and horizontal sweeps. In the advent of an interruption or loss of either or both sweeps the sweep fail signal will disable the high voltage power supply.

A BIT test output is supplied to the BIT test circuitry.

2.8.6 Dynamic Focus/Horizontal Linearity Correction Module

Functional Requirements

Optimum focus is maintained for any position of the CRT spot by applying a parabolic voltage waveform to the grid number four electrode.

Linearity correction is obtained by sampling deflection current and applying a voltage to the yoke in a sense to reduce resistance loss. The yoke then appears as a pure inductance to the deflection system and non-linearity due to yoke losses is removed.

Signal	Number of Lines	Signal Type	Characteristics
Input Interface			
+600V	1	DC Bias	10 MA
Horiz. Deflection	2	Pulse	Horiz. Line Rate
+25VDC	1	Power	50 MA
-25VDC	1	Power	25 MA
Output Interface			
Dynamic Focus	1	Parabolic Waveform	Horiz. Line Rate
Horiz. Linearity Correction	1	Ramp	Horiz. Line Rate
Horiz. Sweep	1	Ramp	Horiz. Line Rate
BIT	1	DC	

Module Functional Description

Dynamic focus is obtained by converting the horizontal sweep to a parabolic wave form and driving grid number four. The waveform is AC coupled and added to the DC potential required for focus depending on the CRT in use.

Horizontal linearity correction is established by sampling the current through the horizontal yoke, converting the sample to a voltage drive and reapplying it to the yoke. The horizontal drive for the sweep fail protection is also generated from this circuit. The functions performed on this module are shown in Figure 32.

A BIT output is provided to monitor the function of the module.

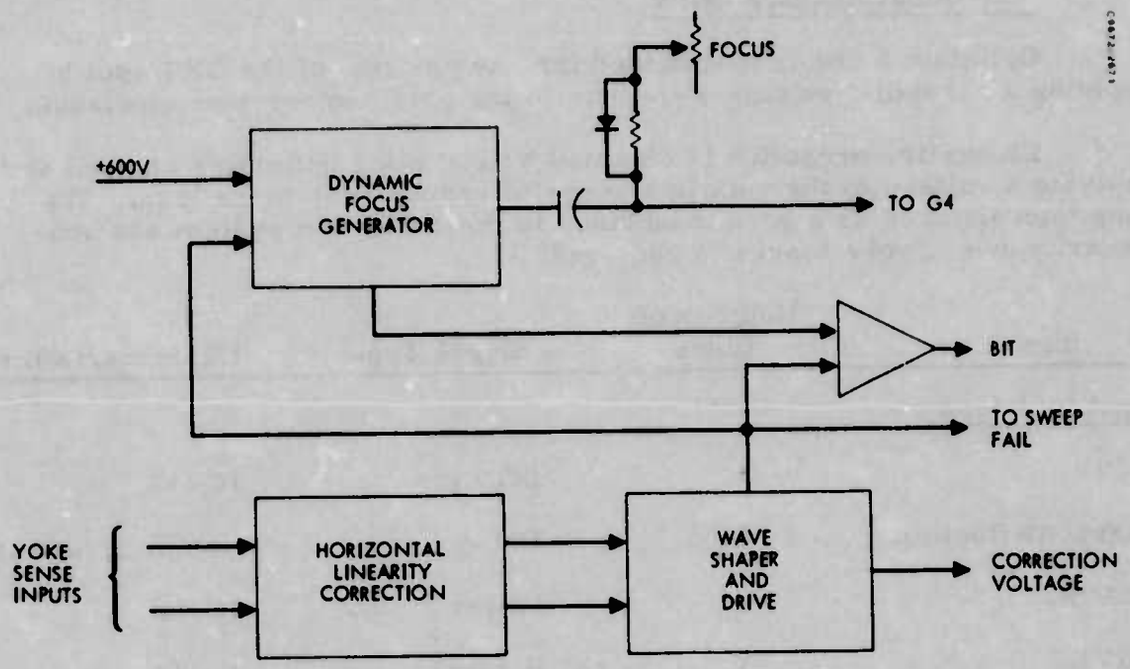


Figure 32. Dynamic focus/horizontal linearity.

2.8.7 High Voltage Power Supply

Functional Requirements

The High Voltage Power Supply is an efficient energy-conversion system which generates all DC voltages required to drive the CRT electrodes. These DC voltages are:

- Anode potential, adjustable from 15 KV to 20 KV depending on CRT
- 110 VDC for the video amplifier and blanking circuits
- 600 VDC for dynamic focus circuit
- 300 VDC for Grid No. 2

Signal	Number of Lines	Signal Type	Characteristics
Input Interface			
Vertical Sync	1	Ramp	60 HZ
Sweep Fail	1	Switched DC -25VDC/Open	
-25VDC	1	Power	1 Amp
Output Interface			
Anode Potential	1	H. V. 15 KV-20 KV Adjustable	DC
110 VDC	1	DC Bias	<10 MA
300 VDC	1	DC Bias	<1 MA
BIT Output	1	DC Voltage Proportional to Anode Potential	

Module Functional Description

The high voltage power supply consists of a power oscillator driving a step-up transformer whose secondary windings are used to generate the DC voltages. Feed-back is provided to insure stability and regulation as shown in Figure 33.

The power oscillator is synchronized to the vertical sweep to insure starting and to phase lock conducted and radiated interference from the power oscillator.

The sweep fail signal disables the high voltage power supply in the advent of a loss of either the horizontal or vertical sweep to protect the CRT phosphor from burning due to the undeflected spot.

A BIT output is provided which is a low voltage pick off from the anode potential.

The high voltage power supply will occupy a volume of not more than 60 cubic inches.

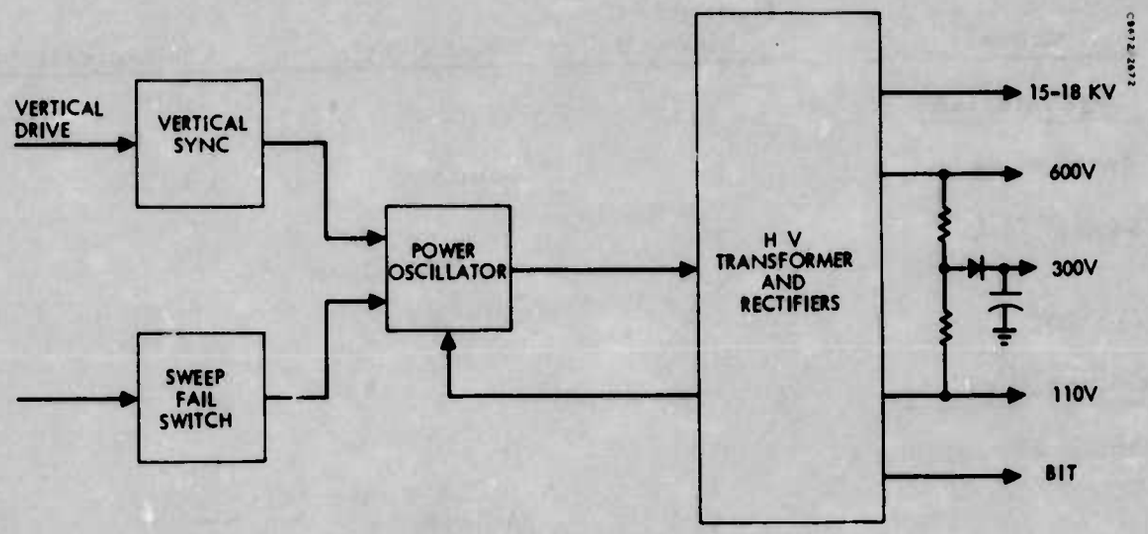


Figure 33. High voltage power supply.

2.8.8 Low Voltage Regulators

Functional Requirements

The low voltage regulators provide the necessary regulated DC voltages required to drive the display circuitry. They are:

- +25 VDC
- -25 VDC
- +5 VDC

The regulators shall also provide over current protection and in the case of a loss of a voltage shall shut down the remaining voltages to protect the display circuitry. A module of this type can also be used in the Digital Signal Transfer Unit, however the voltage and current capability will depend on the application.

Signal	Number of Lines	Signal Type	Characteristics
Input Interface			
+30 VDC	1	Semi-Regulated DC	
-30 VDC	1	Semi-Regulated DC	

(Continued)

(Concluded)

Signal	Number of Lines	Signal Type	Characteristics
+9 VDC	1	Semi-Regulated DC	
Output Interface			
+25 VDC ±2%	1	Power	1A
-25 VDC ±2%	1	Power	2A
+5 VDC ±2%	1	Power	1A
BIT Power Fault	1	Switched DC	+12/Open

Module Functional Description

The low voltage regulators utilize integrated circuit voltage regulators with external pass stages mounted on appropriate heat sinks. The output voltages are sensed for over and under voltage conditions to protect against regulator failure. Internal current limiting is also provided. The regulator function is shown in Figure 34.

The fault detector provides an output which shuts down all DC power forms in the event of a failure. A BIT failure signal is also provided.

The discrete power transformer and rectifier components that generate the irregulated inputs to this module are mounted on the indicator chassis to provide ease in cooling.

2.8.9 BIT Generator/Data Mux

Functional Requirements

The BIT generator/data mux module provides, under control of an external enable signal, an internally generated test signal capable of generating 8 vertical shades of grey on the display in a standard 525 line format.

Bit data is multiplexed via a serial word under the command of the DSTU or DAIS mux bus as shown in Figure 35.

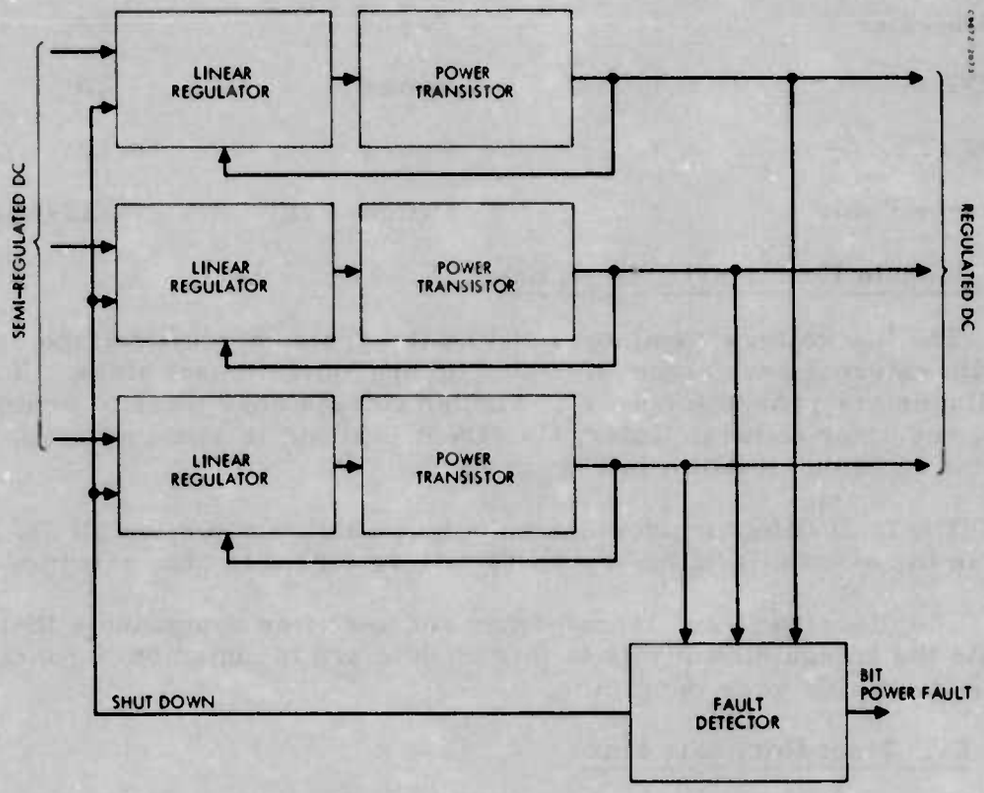


Figure 34. Low voltage regulators.

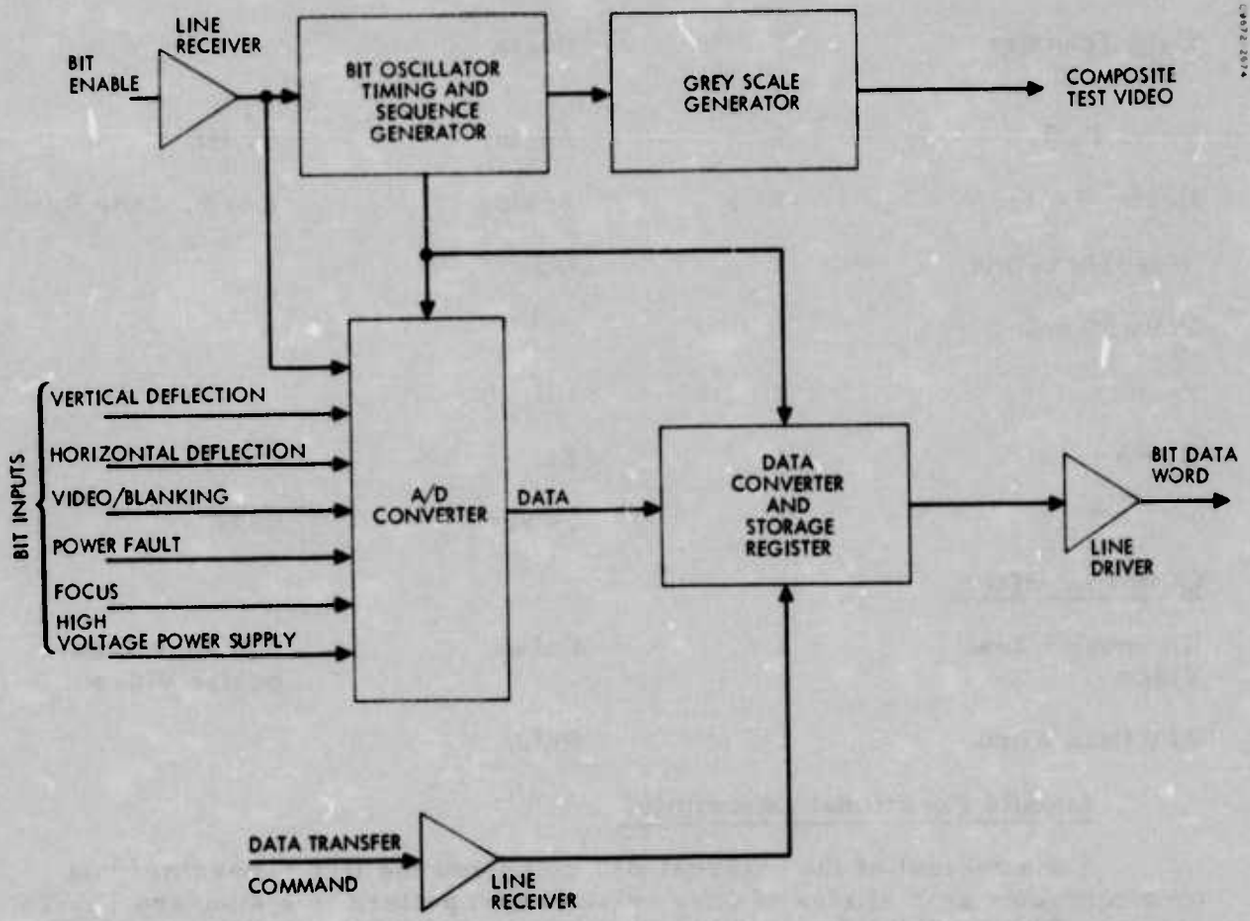


Figure 35. Bit generator/data mux.

Signal	Number of Lines	Signal Type	Characteristics
Input Interface			
BIT Enable	1	Pulse	
Data Transfer Command	1	Pulse	
Vert. Defl.	1	Analog	60 HZ
Horiz. Defl.	1	Analog	Horiz. Line Rate
Video/Blanking	1	DC	
Power Fault	1	Pulse	
Focus	1	DC	
HVPS	1	DC	
+5 VDC	1	Power	0.7A
Output Interface			
Composite Test Video	1	Pulse	525 Line Composite Video
BIT Data Word	1	Pulse	

Module Functional Description

Upon receipt of the external BIT command the BIT generator/data mux generates an 8 shades of grey vertical test pattern in a standard 525 TV format. The composite test video signal is used to generate test conditions in all the function modules of the display which in turn generate their own internal BIT signals. The BIT signals are converted into a serial digital word which is transferred to the DSTU.

Data conversion is done by a multiplexed A/D converter under the control of the BIT timing and sequence generator.

3.0 APPLICATIONS ANALYSIS

3.1 Introduction

In this section the applicability of the modular multi-sensor display system to the various systems described in Section 2.0 is presented. Special interface modules required when the DAIS interface is not available are also discussed.

A specific system application is analyzed in more detail. The specific system selected for analysis is the DAIS baseline, namely the APQ 126 (A-7 radar) with an Electro Optical Sensor freeze mode capability. Four alternate configurations of this system are studied; an analog design, a discrete design using MSI components, the modular design with MSI components and the LSI modular design. These alternates are traded off against such parameters as weight, power, volume, reliability and cost of ownership. This trade off indicates that the modular design is better when successive multiple system buys are anticipated. The LSI version results in a substantial percent cost savings over a discrete digital designed system. It also possesses more than twice the MTBF. A discussion of the cost of ownership analysis is then presented, followed by the derivation of the system reliability estimates. This section is concluded with a description of the physical design of both an MSI and LSI digital signal transfer unit and Multi Mode Display to meet the A-7 O & M configuration.

3.2 Multiple System Applications

3.2.1 General Application

The numbers and types of Signal Transfer Unit modules required to meet multiple system requirement using either the MSI or LSI designed modules are summarized in Tables 11 and 12. The primary differences are in the number of memory modules required. The LSI memory module has a storage capability of 131K bits. This is twice that of the MSI memory module. The total number of MSI memory modules is then twice the LSI figure. The overall amount of memory required is listed in the Summary Requirements Table of Section 3.0 with one additional bit level provided to store symbol information. This memory size is based on the radar scan conversion requirements. If EO sensor freeze is required, either the radar memory can be used as is, or additional memory modules can be added to provide the necessary resolution.

Aircraft with two independent display channels require two memories. For the F-111 series aircraft appropriate memory sizes are provided to accomplish the simultaneous scan conversion of two radar sensors (TF and attack). For the B-1 systems a double memory is also provided to allow simultaneous attack and TF displays. The BI-EAR is assumed to possess a DAIS type interface.

The F-111A, F-111D, FB-111 and B1 require 4 controllers for two separate display channels. Two controllers can control two sensor channels and two separate symbol generator controllers are required. These systems then have two completely independent display channels.

The F-4D, F-4C, F-4E, and F-106, have two displays but only one scan conversion channel is required. Thus, only one scan converter controller and one symbol generator controller are needed. Even with this limited system one display can present TV or FLIR while the other display presents radar video. However, simultaneous freeze of the EO video cannot be achieved while scan converting the radar video. If these functions are required simultaneously, a larger memory and additional input and output modules are required.

3.2.2 Special Interface Modules

The number of interface modules listed in the LSI and MSI Module Tables indicate the special module design effort required for retrofit into these aircraft systems where the DAIS interface is not available, these modules are needed to convert antenna and control signals into the appropriate digital words for use in the Modular Multi-Sensor Display System. Essentially they convert non-DAIS interface signals into the DAIS digital parallel word format.

For the F-4 series aircraft, three interface modules are required. An analog to digital module is needed to convert Symbol Translation and Position analog signals. A synchro to digital resolver is needed to convert the sine and cosine values of the antenna pointing angle for PPI display. And last, a high level to low level logic converter is needed to convert 28 volt signal into 5 volt TTL levels.

The F-106 aircraft system also requires three interface modules similar to the F-4. An A/D module is needed for control position signal conversion. The IRST interface in this system is the receiver for the IR video. The IR detector is slaved to the radar antenna, hence the radar antenna position signals can be used.

The F-111 series aircraft employ a unique digital interface. It is assumed that two digital modules can be used to accept and convert the sensor and symbol information for use in the modular system.

A-7 aircraft require three interface modules. An A/D module, a 400 Hz demodulator for azimuth and a control signal Mode Logic Decoder. A-7 aircraft converted to a DAIS interface would not require these modules.

The F-15, as does the F-111, uses a special digital interface and needs a digital interface module. Applicability of the modular system to F-15 would provide an improved ground mapping capability and would be desirable if the role of the F-15 was expanded to encompass air-to-ground weapon delivery.

	F-4C	F-4D	F-4E	F-106	A7D
	APQ100	APQ109	APQ120	MA1	APQ126
Number of Displays	2	2	1	1	1
Display Video Channels	1	1	1	1	1
1. Receiver, A/D	1	1	1	1	1
2. Input Processor Memory	1	1	1	1	1
3. Input Processor Logic	1	1	1	1	1
4. Controller	2	2	2	2	2
5. Controller Memory	1	1	1	1	1
6. Refresh Memory (131K)	4	4	4	2	4
7. Input Address Gen.	1	1	1	1	1
8. Output Address/Sync Gen.	1	1	1	1	1
9. Output Video Processing	1	1	1	1	1
10. GP Clock Gen.	1	1	1	1	1
11. Symbol Gen. List Decoder	1	1	1	1	1
12. Chain Gen.	2	2	2	2	2
13. Special (Clock Function, Blanking)	1	1	1		2
14. Interface	3	3	3	3	3
Total	21	21	21	18	22

TABLE 11. LSI MODULE APPLICABILITY

A7D	F-111A		FB-111		F-111D		F-15	B-1	
APQ126	APQ113 Attack	APQ110 TF	APQ114 Attack	APQ134 TF	APQ130 Attack	APQ128 TF	APG63	F111 Avionics	EAR
1	1	1	1	1	1	1	1	2	2
1	1	1	1	1	1	1	1	2	2
1	1	1	1	1	1	1	1	2	2
1	1	1	1	1	1	1	1	2	2
1	1	1	1	1	1	1	1	2	2
2	2	2	2	2	2	2	2	4	4
1	1	1	1	1	1	1	1	2	2
4	6	3	6	3	6	3	2	9	26
1	1	1	1	1	1	1	1	2	2
1	1	1	1	1	1	1	1	2	2
1	1	1	1	1	1	1	1	2	2
1	1	1	1	1	1	1	1	2	2
1	1	1	1	1	1	1	1	2	2
2	2	2	2	2	2	2	2	4	4
2	2	2	2	2	2	2	1	4	3
3	2	2	2	2	2	2	1	4	0
22	43		43		43		17	43	55

	F4C	F4D	F4E	F106	A7D	F-111A	
	APQ100	APQ109	APQ120	MA1	APQ126	APQ113	A
Number of Displays	2	2	1	1	1	1	
Display Video Channels	1	1	1	1	1	1	
1. Receiver, A/D	1	1	1	1	1	1	
2. Input Processing Memory	1	1	1	1	1	1	
3. Input Processor Logic	1	1	1	1	1	1	
4. Controller	2	2	2	2	2	2	
5a. Sensor Controller Memory	1	1	1	1	1	1	
5b. Symbol Generator Memory	1	1	1	1	1	1	
6. Refresh Memory (65K)	8	8	8	4	8	12	
7. Input Address Gen.	1	1	1	1	1	1	
8. Output Address/Sync Gen.	1	1	1	1	1	1	
9. Output Video Processing	1	1	1	1	1	1	
10. GP Clock Gen.							
a. Input	1	1	1	1	1	1	
b. Output	1	1	1	1	1	1	
11. Symbol Gen. List Decoder	1	1	1	1	1	1	
12a. Chain Gen, X	1	1	1	1	1	1	
12b. Chain Gen, Y	1	1	1	1	1	1	
13. Special-GSC and/or TF, Blanking	1	1	1	0	2	2	
14. Interface	3	3	3	3	3	2	
Total	27	27	27	22	28		56

TABLE 12. MSI MODULE APPLICABILITY

A7D	F-111A		FB-111		F-111D		F15	B-1	
Q126	APQ113	APQ110	APQ114	APQ134	APQ130	APQ128	APG63	W/F111 Avionics	TF and Attack EAR w DAIS
1	1	1	1	1	1	1	1	2	2
1	1	1	1	1	1	1	1	2	2
1	1	1	1	1	1	1	1	2	2
1	1	1	1	1	1	1	1	2	2
1	1	1	1	1	1	1	1	2	2
2	2	2	2	2	2	2	2	4	4
1	1	1	1	1	1	1	1	2	2
1	1	1	1	1	1	1	1	2	2
8	12	6	12	6	12	6	4	18	51
1	1	1	1	1	1	1	1	2	2
1	1	1	1	1	1	1	1	2	2
1	1	1	1	1	1	1	1	2	2
1	1	1	1	1	1	1	1	2	2
1	1	1	1	1	1	1	1	2	2
1	1	1	1	1	1	1	1	2	2
1	1	1	1	1	1	1	1	2	2
2	2	2	2	2	2	2	1	2	3
3	2	2	2	2	2	2	1	2	0
8	56		56		56		21	52	84

The B-1 systems are also to be all digital systems and may incorporate a DAIS type interface, therefore, no special interface would be required. In the first B-1 systems with a modified F-111 avionics system the special interface requirements will match those of the F-111's.

Table 13 lists the types and respective quantities of modules needed in the CRT Monitor Indicators of the various aircraft systems. The numbers and type of modules required reflect the appropriate CRT sizes (based on existing display O&M) and the number of separate displays in the systems.

3.3 Specific System Applicability

To determine the relative merits of using the modular display system described and designed in this report, it was compared with other more traditional display system alternates. The APQ 126 (A7) radar system was selected as the system for comparison because it possesses dual TF/ATTACK radar mode capability and is probably the system to be incorporated in the Air Force hot bench DAIS brassboard. As a base line, this system must provide scan conversion of all the radar formats and necessary attack symbology. Also an EO Freeze capability is assumed. This freeze capability essentially comes for free, (no added modules) except for the non-recurring cost of controller programming. The APQ 126 radar requires a memory of 512 x 256 x 3 bits which will also be used for the EO freeze. In the event that an EO Sensor with 875 lines is employed either the existing memory can be used to freeze a portion of the area or more memory can be added. Also, it is assumed that the DAIS interface will be employed. Therefore, none of the special interface modules are used. Four alternate display system configurations were evaluated; an analog display system, a discrete digital design, and the LSI and MSI modular designs. Each alternate is briefly described in the following paragraphs.

The first alternate is an analog scan converter system. The actual tradeoff numbers derived are based on a previous Hughes analog scan converter systems analysis. Also an analog symbol generator design was assumed to meet that requirement for the A7 application.

The second alternate is a design specifically tailored to the A7 display requirements. State-of-the-art digital and analog circuits are employed and hardwired timing and control circuitry is used. This design was based on a Hughes response to an RFP (1972) to develop a digital display system for the A-7.

The third and fourth alternates are the use of the MSI and LSI modules designed in Section 5.0 for the A-7 application. They possess the same basic block diagrams as presented in Section 5.0 with the module complements shown in Tables 11, 12 and 13 for the A-7. The only two special modules required are the special clock generator module to generate the TF and ground range clocks and an out of scan blanking generator module. No special interface modules are required since the DAIS interface is assumed.

TABLE 13. INDICATOR MODULE APPLICABILITY

	All F-4s	F-106	A-7D	All F-111s		F-15	B-1
				Attack	TF		
CRT, No., size, in. (Special)	2	1	1	1	1	1	2
	(5)	(5)	(5)	(8)	(8)	(5)	(8)
Vertical Deflection Amplifier	2	1	1	1	1	1	2
Horizontal Deflection Amplifier	2	1	1	1	1	1	2
High Voltage Power Supply	2	1	1	1	1	1	2
BIT Generator Data Mux	2	1	1	1	1	1	2
Video Amp, Blanking	2	1	1	1	1	1	2
Dynamic Focus, Horiz. Linearity	2	1	1	1	1	1	2
Power Trans. Rectifier, Filter	2	1	1	1	1	1	2
Power Regulator	2	1	1	1	1	1	2
Total Indicator Modules	18	9	9	9	9	9	18

All four systems are assumed to consist of 2 units, a signal transfer unit (scan converter and symbol generator) and indicator unit. Also, for the sake of comparison, the indicators are assumed to be physically and functionally identical (multiple line television format compatible). The only exception to this is in the area of cost of ownership since only in the modular systems can it be assumed that essentially off the shelf display modules (designs) are available for incorporation in subsequent system applications.

The parameters upon which the four alternates were compared are weight, power, volume, module number, reliability, maintainability, and cost of ownership. The results of this tradeoff are shown in Table 14. Performance is considered to be equal for all three digital scan converter alternates. The analog scan converter is considered unacceptable due to its low reliability, maintenance problems, and sensitivity. Also it is too large for the existing A-7 transfer unit space. The weight and volume numbers are derived from the required packaging configuration to meet the A-7 requirement. Both the discrete and MSI modular design can meet this requirement. Physical descriptions of both modular systems are presented in Section 6.6. The LSI version can be packaged in an even smaller unit. The relative cost of ownership estimates are total ten year costs, based on three successive buys (250 each) of systems of essentially the same complexity spaced 2 years apart. This analysis and the reliability analyses are discussed in more detail in following sections of this report.

The Mean Time To Repair estimates are best engineering estimates for the intermediate level repair of the various alternate configurations. The estimate of 4 hours for the analog system assumes that approximately half of the failures require replacing of the tube, which is an 8 hour job. The other failures dictate circuit board or module replacement which can run up to 1 hour MTTR. The 1 hour MTTR estimate was also used for the discrete design digital system. The modular design because of the unique capability of the controller to provide instant isolation of failure to the module level should be repairable in approximately 0.5 hour. The digital systems also possess significantly fewer maintenance adjustments than an analog system.

As can be seen from the table, the MSI modular system does cost slightly more than a discrete design in the first system procurement. This is partly due to a higher design cost and the larger number of components (circuit card/modules) necessary for its implementation. If however, a second system application comes along, the basic core modules can be used. The only new R & D costs are for the packaging, reprogramming of new modes/symbology, and the design and development of new interface modules (if required, assuming a non-DAIS interface). Module production costs are reduced due to larger production quantities of identical modules.

The LSI version of the modular system promises to provide even lower cost, and improved reliability. The MTBF of the LSI implemented system is over twice that of MSI. This is due to the inherent high reliability of LSI circuitry (monolithic circuits, minimum interconnects, etc.). The lower cost is due partly to the improved reliability and partly due to the lower high volume production price of LSI. Additional cost benefits not

TABLE 14. ALTERNATE DISPLAY SYSTEM CONFIGURATION TRADEOFF

	Analog/Scan Converter/Symbol Generator			Discrete Digital Design			Modular MSI Design			Modular LSI Design		
	STU	DISP	TOT	DSTU	DISP	TOT	DSTU	DISP	TOTAL	DSTU	DISP	TOT
Performance	Fair			Good			Good			Good		
Weight, lbs	45	20	65	25	20	45	27	20	47	20	20	40
Power, watts	160	130	290	220	130	350	270	130	400	270	130	400
Volume, cu ft	0.9	0.35	1.25	0.35	0.35	0.70	0.35	0.35	0.70	0.35	0.35	0.70
Adjustments	35	6	41	2	6	8	2	6	8	2	6	8
Card Module Size, in	NA			5.6 x 6.2			5.6 x 6.2			4.7 x 4.1		
Number of modules				20	9	29	25	9	34	19	9	28
MTBF, hrs	200	3100	190	1010	3100	765	850	3100	670	4850	3100	1890
MTTR, hrs			4			1.0			0.5			0.5
Cost of ownership (Relative) (10 yr, 250 system buys) (accumulative total)												
1st System			1.7			1.0			1.1			1.0
2nd System			3.4			2.0			1.9			1.7
3rd System			5.1			3.0			2.6			2.3
Conclusion	Unacceptable									Preferred after MSI Brassboard is operating		

analyzed could be accrued in the Air Forces' logistics and maintenance structure making the modular display system even more attractive. The LSI modular display system is recommended with the provision that a brassboard model of all modules be operating in a system prior to committing to LSI fabrication.

3.4 Cost of Ownership Analysis

This cost of ownership analysis is addressed primarily to the general discussion of factors in the cost study – including (a) the identification and general description of the various cost elements and (b) equipment reliability and how it affects the total life cycle cost. This is followed by a cost table which summarizes the specific analysis performed.

Operational support costs summarized herein were predicted using the procedures and cost values described in AFLC/AFSCM 800-4, "Optimum Repair Level Analysis" (ORLA), dated 25 June 1971, supplemented by more up-to-date information where available, and modified for specific applicability to this study.

The maintenance concept includes all the necessary support equipment and services to sustain the systems at all three basic levels of maintenance: organizational, intermediate (field) and depot.

Organizational level maintenance is considered to be any maintenance which is performed on the equipment in its operational environment, and does not require detailed disassembly nor complex external test equipment. This is considered to be limited to removing a faulty line replaceable unit (LRU) from the aircraft, delivering it to the repair shop for further maintenance, and installing a good unit in its place.

Intermediate (field) level maintenance is that maintenance performed in a repair shop, normally on the base to which the equipment is assigned. Repair at this level consists of repairing an LRU by replacement of a faulty module, using field shop AGE for fault isolation to the module level, and verification of repair.

Depot level maintenance is that which is beyond the capabilities of organizational and field levels. Tasks performed at this level are of a technically complex nature and require more sophisticated facilities, support equipment, and highly skilled personnel which may not be available at the field level. Repair of faulty modules, or repair of an LRU when fault isolation does not detect a failed module, are examples of the repair tasks of the depot.

The total cost of ownership of a block of hardware systems in a given inventory can be considered to be composed of two major elements: (1) acquisition costs and (2) operational support costs. The first covers the contractor development costs and the customer initial procurement cost. The second covers all items required to keep the system operational through the total

life of the systems. The total cost of ownership can thus be expressed as

$$TCO = AC + OSC$$

where:

TCO = Total life cycle cost (total cost of ownership through the total life of the system

AC = Acquisition cost

OSC = Operational Support cost.

3.4.1 Acquisition Cost

Acquisition cost (AC) is the sum of various non-recurring cost elements which can be expressed as

$$AC = C_{cd} + C_p + C_i + C_a + C_t + C_{as} + C_d + C_f + C_{fs} + C_r$$

where·

C_{cd} = Contractor developmental costs including all engineering costs and documentation required for production.

C_p = Cost to the customer for the block of production systems.

C_i = Contractor costs associated with production implementation.

C_a = AGE cost consists of costs for all system test and diagnosis equipment at depot and intermediate levels, including engineering and fabrication of one set of test equipment at each repair facility. Also, included is the cost of diagnostic software (computer cost and programming manpower).

C_t = Training Cost - includes manpower for training equipment operators and maintenance personnel at all levels, and includes training aids, which, as a minimum, will include one set of production hardware. It is assumed that all personnel to be trained for initial operational support capability will be trained at a single location.

C_{as} = Acquisition spares cost - the cost of the initial inventory of spares required to assure a specific confidence level of having the required number of spares available at the using facility when needed. A 90 percent confidence level has been utilized in this cost estimate.

C_d = Technical data cost - includes the cost of all publications required to support the operation and maintenance of all equipment at all levels.

C_f = Facilities cost - includes the cost of any unique requirements necessary for adequate operation and maintenance of the equipment and/or service equipment, primarily at the intermediate and depot levels. For this study no special facilities are anticipated to be required in addition to those already existing to support other equipment at the same locations.

C_{fs} = Field Support cost - includes contractor effort in assisting the various field operation levels as required, to provide initial operational support capability.

C_r = Retrofit cost - no retrofit costs are assumed in this cost estimate.

3.4.2 Operational Support Cost

Operational Support Cost (OSC) is the sum of various recurring cost elements which can be expressed as

$$OSC = C_m + C_{rs} + C_{am} + C_{ps} + C_{sa} + C_s + C_{fm} + C_{rt}$$

where:

C_m = Manpower cost - (repair labor) - includes the cost for time spent on repair and/or replacement of faulty hardware at the intermediate and/or depot levels, and cost for LRU replacement at the organizational level. Repair labor time includes only that time required for fault isolation, repair or replacement, and subsequent verification of proper operation.

C_{rs} = Replenishment spares cost - includes costs of all subassemblies, modules and parts used in the repairs performed at the intermediate and depot level.

C_{am} = AGE maintenance cost - includes costs associated with the general maintenance and repairs of test equipment at the intermediate and depot levels over the life cycle.

C_{ps} = Packaging and Shipping cost - the cost of two-way transportation from field base to depot when a decision is to repair a certain item at depot level, and the cost of one-way transportation from depot to field base when the decision is to repair at the intermediate level.

C_{sa} = Supply administration cost - cost of maintaining non-standard parts and assemblies introduced into the customer inventory, computed over the life cycle.

C_{s} = Space - includes any additional space requirements required to accommodate the system maintenance operation. This study assumes no additional requirements for new space.

C_{fm} = Facilities Maintenance - includes the cost of maintenance of any new and/or special facilities required for the system maintenance. Since no additional facilities are necessary, this value is zero.

C_{rt} = Replacement training cost - the cost of training new (replacement personnel at all operational levels during the total life cycle.

Table 15 presents a cost of ownership comparison of the four A-7 display systems previously described. The estimate is projected to cover the procurement of three blocks of systems, each for a new similar application, of 250 systems each made at two year intervals.

The two modular systems (MSI and LSI) consist of the modules described in Section 2.0 of this report. The basic feature in this design is that it presents a set a standard "building blocks" which can be used in various combinations and quantities to achieve the required system for any application. With this design it is only necessary to customize the unit chassis to fit the particular installation requirements. The "off-the-shelf" modules would then "plug-in" to the custom chassis. Development costs of this type system would be confined to the chassis, reprogramming and interface costs. No additional engineering costs would be incurred for core module design. Future savings would also be realized in system production costs due to the larger production quantities of identical modules.

The "discrete design" uses the same type components as the modular MSI design except that it does not use a modular approach. Each application would be a total custom redesign wherein the chassis and all its subassemblies would be designed each time to fit the particular required envelope. Complete engineering development costs would be incurred for each different system design. In addition, it is unlikely that production costs would reflect any savings as a result of previously produced systems.

The analog system assumes a new design with each successive buy just as the discrete digital design. However, the low reliability and high cost of the analog scan converter tube results in a very high operational support cost. This is not considered a viable alternate for this application.

The discrete digital design appears to have a slightly lower cost of ownership than the modular MSI for a single buy. This is due to the slightly increased complexity of the modular MSI system to permit multiple application

TABLE 15. RELATIVE TOTAL COST OF OWNERSHIP ANALYSIS

System Block Purchase	Analog System			Discrete Design			Modular MSI			Modular LSI		
	1	2	3	1	2	3	1	2	3	1	2	3
Acquisition (non-recurring) development, production, spares, factory implementation	0.92	0.91	0.90	0.95	0.94	0.93	0.99	0.73	0.66	0.92	0.63	0.54
Operational support costs (recurring, 10 years)	0.79	0.79	0.79	0.06	0.06	0.06	0.07	0.06	0.05	0.08	0.07	0.06
Total	1.71	1.70	1.69	1.01	1.00	0.99	1.06	0.79	0.71	1.0	0.70	0.60
Accumulated Costs	1.71			1.01			1.06			1.0		
	3.41			2.01			1.85			1.70		
	5.10			3.00			2.56			2.30		

integration. Future buys indicate a lower cost for both modular systems. The LSI version is better than the MSI version since it is cheaper than the discrete design even in the first procurement. By the third procurement the accumulated savings approach 25 percent. The third procurement cost itself is 60 percent of the discrete design. These savings result from lower production cost and improved reliability. However, there is a risk factor with LSI due to the advanced technology employed and the possibility of "infant mortality" effects on the MTBF with the subsequent increase in the operational support costs. This factor is not reflected in the table. It is highly recommended that a complete MSI brassboard be operating prior to committing to the LSI design.

This analysis assumed no modification in the Air Force's logistics and training philosophy, therefore the operational costs of all digital systems are almost identical. The modular approach offers the possibility of further cost savings in the future through changes in operational support logistics. If several systems employing identical modules were serviced at the same base, a common maintenance operation could be employed thereby reducing some of the nonrecurring acquisition costs and some areas of the operational support recurring costs. It can be concluded from this analysis that the MMSDS concept is highly desirable from a cost of ownership standpoint.

3.5 Reliability Analysis

Reliability plays a significant role in the system life cycle cost. As system reliability increases, costs naturally decrease. Acquisition spares cost would decrease since fewer assemblies and parts would be required to assure the required level of confidence of having repair parts available at the using facility when needed. Likewise the cost of replenishment parts would be reduced along with a significant reduction in repair labor costs at maintenance levels. The space and handling of inventory spares would also be less, since less parts would be required.

The MMSDS MSI system analysis is presented below. The reliability estimates of the other alternates were made in the same manner.

The system is assumed to be composed of non-redundant components. The system failure rate thus represents the gross sum of the failure rates for all modules and the parts contained therein. The units are series risk functions and the mathematical computation is that of a simple series system without redundancy or degraded modes.

A series risk mathematical model for the reliability prediction for the modular MSI version of the DSTU was generated using the following list of parts and their estimated failure rates. The parts list was derived from the detail module design. For simplification, the total parts count for the application (APQ 126) is used rather than repetitively listing a module by module breakdown. In either method of calculation, the total unit MTBF is identical.

Component	Number of Parts	Failure Rate, Percent/10^3 Hours
Memory IC's (4K Bit)	128	0.42%
Other IC's	972	0.055%
Transistors/diodes	125	0.02%
Resistors/capacitors	250	0.01%
Modular power supply	1	5.0%
Chassis wiring, connectors, circuit boards, wire wrap plate, etc.	1	0.5%

The DSTU failure rate is thus calculated as follows:

$$\begin{aligned} \text{DSTU} &= 128\,(0.42) + 972\,(0.055) + 125\,(0.02) \\ &\quad + 250\,(0.01) + 5.0 + 0.5 \\ &= 53.76 + 53.46 + 2.5 + 2.5 + 5.0 + 0.5 \\ &\quad + 117.72 \text{ percent}/10^3 \text{ hours} \end{aligned}$$

$$\text{MTBF} = 850 \text{ hours}$$

A similarly constructed math model for the "Discrete" DTSU, having less parts due to its implementation for a single specific application, shows that the total failure rate DSTU (Discrete) is predicted at 99 percent/10^3 hours. This results in an MTBF of 1010 hours.

Likewise, a math model was constructed for the LSI version of the modular DSTU. However due to the advanced technology involved with LSI devices, a much more complex series of calculations was required. This model was the object of a separate study. Its results were modified to fit the parameters of this cost analysis, resulting in a predicted failure rate for early production units of 20.6 percent/10^3 hours. Thus an MTBF of 4850 hours is predicted for the LSI "DSTU".

To show the predicted reliability for a total display system, a similar reliability prediction was made for a display unit consisting of a five inch CRT display and its associated circuitry. The result of this math model was a failure rate of 32.2 percent/10^3 hours which relates to an MTBF of 3100 hours.

3.6 Unit Physical Descriptions

3.6.1 MSI DSTU Physical Description

The MSI version of the modular digital signal transfer unit, consisting of modules and a power supply, can be tailored to fit the specific requirements of alternate systems. The 25 modules configured to fit in the A-7 signal transfer unit are shown in Figure 36. The MSI discrete design also fits in this form factor since it possesses only 20 card modules. This form factor can, however, be varied within the constraints necessary to provide assembly and maintenance accessibility.

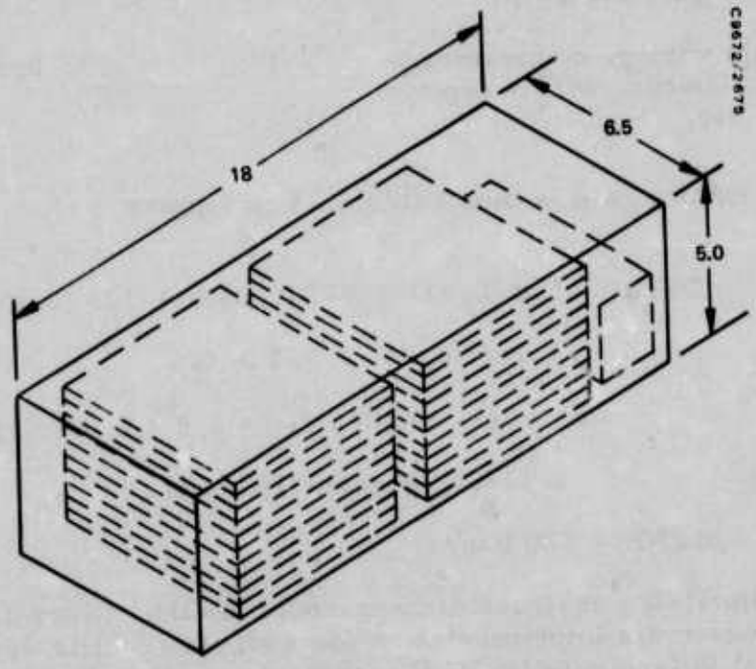


Figure 36. MSI configuration for A-7.

The "basic box" outline includes adequate space for full compliance with environmental requirements Unit covers and connectors are gasketed and power lines filtered as necessary to achieve the required level of EMI/RFI protection. Thermal management is achieved by utilizing forced air cooling provided by a blower located within the unit. The air intake and exhaust openings contain RFI filters.

Installation features of the "basic box" can be tailored to the specific application requirements. Mounting provisions, including the method of attachment and location of attachment points, can be arranged as required. The unit connectors, air intake, and exhaust ports can also be located as desired, with the preferred locations being the ends of the unit.

The basic card module, which is a multi-layer printed circuit card with single side component mounting, is approximately 5.6 inches wide by 6.25 inches high, including the card connector. The module contains a

maximum of sixty (60) integrated circuits and has approximately 100 input/output pins. The "plug-in" card modules mount in a card file which is wired utilizing the "wire-wrap" technique. A modular low voltage power supply is independently mounted adjacent to the card racks as shown in the figure.

3.6.2 LSI DSTU Physical Description

The A-7 modular digital signal transfer unit, consisting of 19 LSI card modules and a power supply assembly, is shown in Figure 37. If necessary even a smaller configuration could be achieved with the LSI modules. This is due to their smaller size and number.

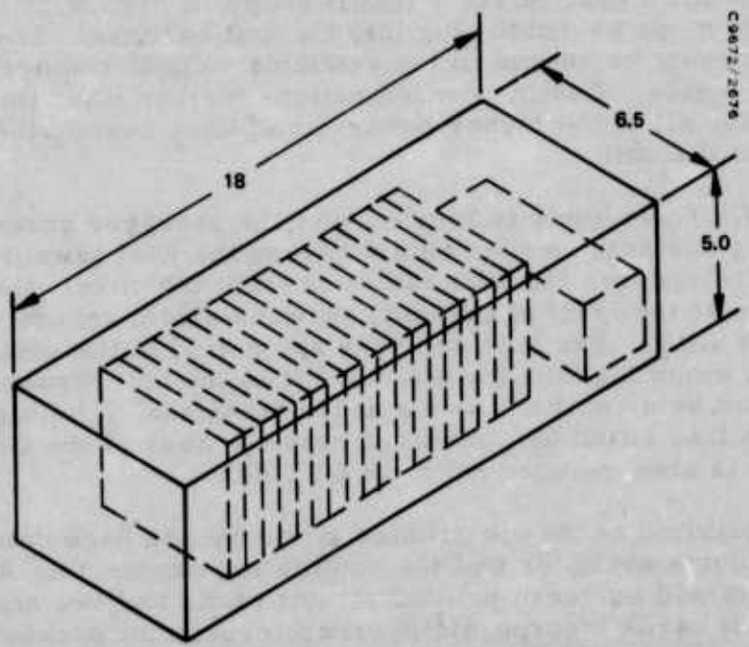


Figure 37. LSI configuration for A-7.

The "basic box" outline includes adequate space for full compliance with environmental requirements. Unit covers and connectors are gasketed and power lines filtered as necessary to achieve the required level of EMI/RFI protection. Thermal management can be a greater problem than the MSI design since the LSI unit volume can be less. It is achieved by utilizing forced air conduction cooling, with the air passing through the cores of the card modules.

Installation features of the "basic box" can be tailored to the specific application requirements. Even more flexibility is achieved due to the small size of the LSI modules. Mounting provisions, including the method of attachment and location to the attachment points, can be arranged as required. The unit connectors, air intake, and exhaust ports can also be located as desired, with the preferred locations being the end of the unit.

The LSI card modules contain a multi-layer printed circuit board with a hollow center core for conduction cooling. Two types of card modules are used: one contains LSI wafers mounted on one side of the card module and the other type contains hybrid components where parts can be mounted to both sides of the card. The "plug-in" card modules mount in a card file containing air plenums for cooling. The card rack is wired using the "wire-wrap" technique. A modular low voltage power supply is independently mounted adjacent to the card rack as shown in the figure.

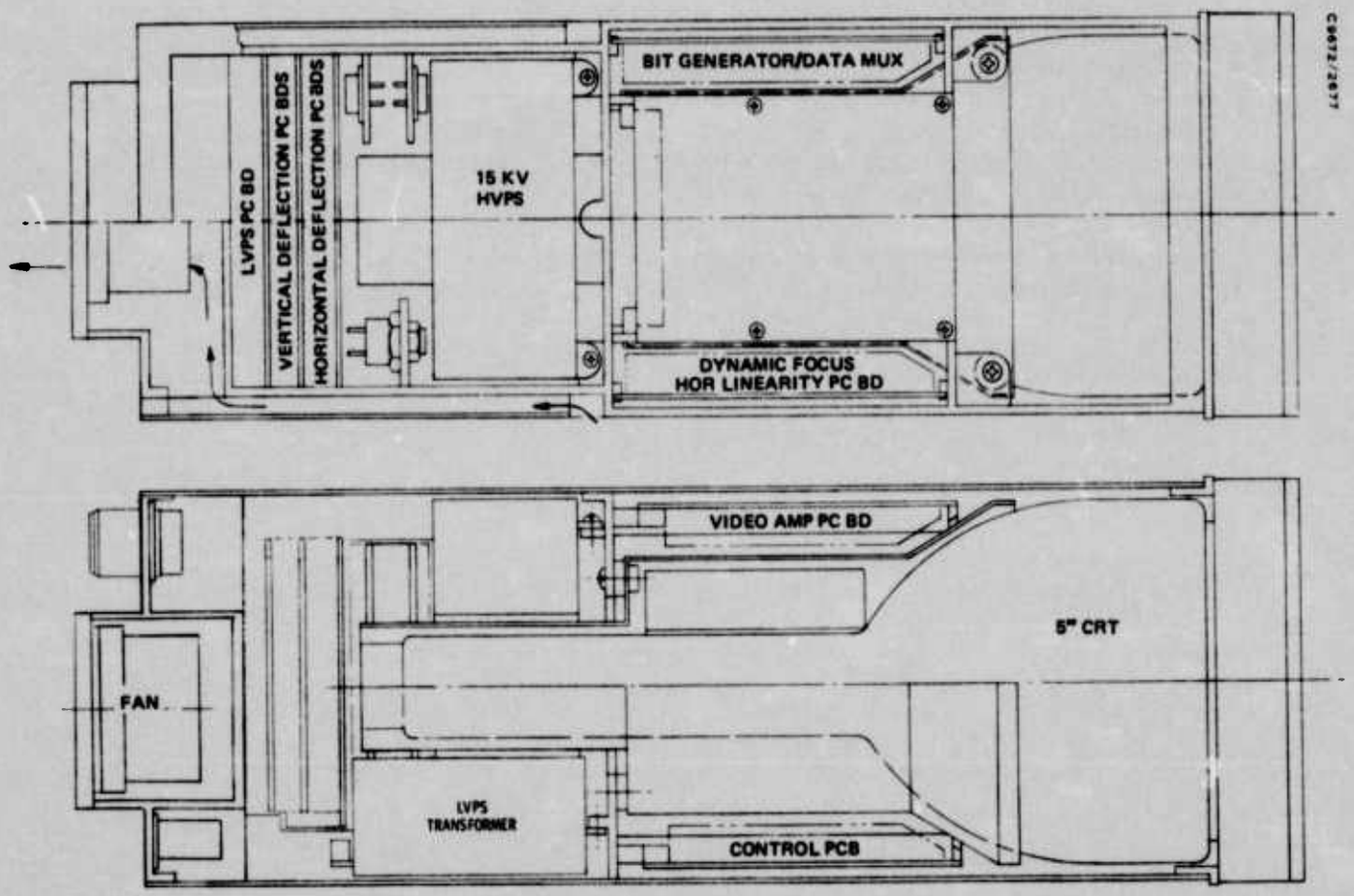
3.6.3 Multi Mode Indicator Physical Description

The Multi Mode Indicator (MMI) shown in Figure 38 has been designed with modules which plug into the unit harness. The number of modules that must be housed in the available volume requires efficient utilization of the space. Cooling considerations further limit the packaging design because all of the higher power dissipating assemblies must be located at the rear of the unit.

The CRT assembly is located with the phosphor screen at the specified unit mounting surface. A tube shield covers the EMI sensitive neck and gun of the tube and reduces the EMI radiation from the yoke. Because of the limited space at the front of the unit, the tube shield covers only the rear portion of the CRT. The tube and yoke are potted in the shield. The shield is fitted with mounting tabs for attaching it to the unit structure. The tube is also supported by a resilient mount at the faceplate. The high voltage power supply is a potted assembly, mounted near the neck of the CRT. The LVPS transformer is also mounted near the CRT neck.

The location of the electronics circuitry has been determined by the remaining volume available and the cooling requirements. All of the circuitry is contained on seven printed circuit cards and two heat sinks. The printed circuit cards incorporate hybrid microcircuit packages and discretes components. The low power electronics have been functionally partitioned on four conventional printed circuit boards, mounted on the sides of the CRT shield, in proximity to the yoke. The remaining three modules, containing the low voltage regulators and deflection circuitry, are mounted in the vicinity of the cold wall. The associated high power discrete components are mounted on finned heat sinks which are attached to the cold wall over a large area. At the rear of the unit is the blower and plenum which provides suction for the cold walls. The remaining unit volume has been used for connectors and harness routing.

The controls for the display are mounted in the removable front end housing, which also contains the curved ambient control filter. This housing is designed to plug into the main housing to facilitate easy removal. The control PCB is a special module provided to digitize and multiplex the control signals onto the DAIS data bus. The signals are then interpreted by the DSTU and balance of the system as required.



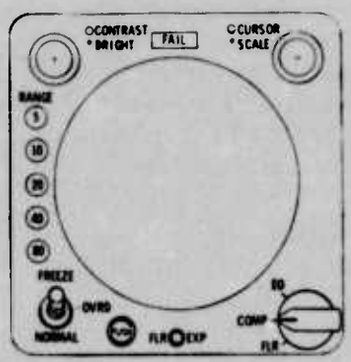


Figure 38. Multi-mode indicator for A-7 aircraft.

APPENDIX A

HUGHES PAD RELOCATION LSI

The Pad Relocation approach to LSI allows circuits on full wafers of varying yield patterns to be interconnected as if all were good. This is accomplished by relocating pads of nearby unused good circuits to replace circuits not passing probe tests.

The Hughes development of the Pad Relocation interconnection technique was undertaken to extend LSI's advantages from complex single chips to entire semiconductor wafers. Pad Relocation or a discretionary routing technique is necessary for this extension since the semiconductor wafer cannot be processed entirely free of defects. Pad relocation is illustrated in Figure A-1, which shows the steps in the fabrication process. In pad relocation, processing through the first metalization layer is common to that of normal integrated circuit processing, except that a mix of circuit cell types is usually included on each wafer.

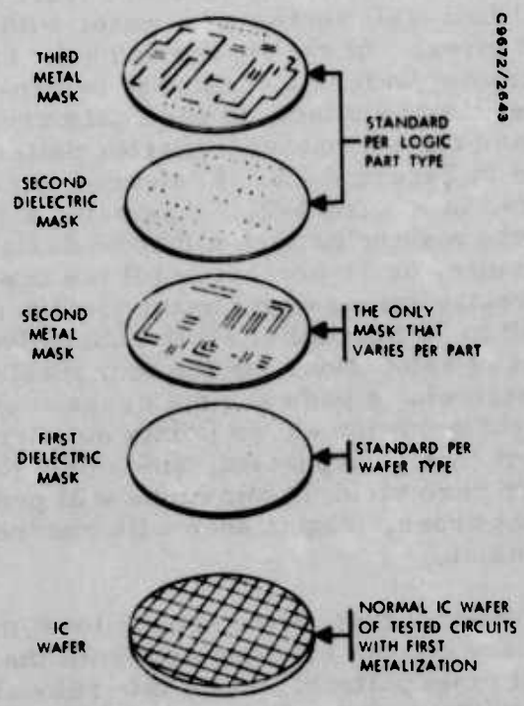


Figure A-1. Multi-level processing stages for low cost, high complexity LSI using pad relocation techniques.

To facilitate subsequent processing, pad locations and cell sizes are made uniform. The two subsequent metalization layers accomplish the required logic circuit connections for the specified design. They also accomplish relocation of the connection pads of the operational circuits to the pre-positioned master pattern pad via locations.

Interconnection between assumed good circuit "master pattern" positions are routed once by computer. One complete and one fractional layer are used for this. The remaining fraction of a layer is used to "relocate" pads of nearly unused good circuits to any master pattern position whose circuit did not pass automatic probe test.

This technique has evolved a low cost means of accomplishing large scale integration on pre-diffused wafers of standard circuit types. The master pattern positions are fixed for any one logic part (wafer) type; all logic routing is identical for all parts produced of that type. Only relocation patterns (a fraction of a metallization layer) differ as a function of the cell yield pattern. Consequently, computer routing to accommodate all necessary relocations for a wafer is a very samll part of the array's production cost, even for wafers with circuit yield as low as 20 percent.

A set of pad relocations is depicted in Figure A-2. Figure A-2a shows a hypothetical four-cell section of a wafer with each cell containing two two-input NAND gates. (In reality the 0.080 by 0.160 inch cells on present 2.2 inch diameter wafers incorporate 16 two-input NAND gates per cell.) The first level metal contacts to each gate are shown schematically as the open circles and the second level master pattern contacts are diagrammed as squares in Figure A-2a. Preferred and alternate relocation patterns are suggested in Figure A-2b. Assuming a 70 percent typical gate yield at probe test, the master pattern might be designed as shown to use 50 percent of all circuits, or 71 percent of all the expected operative circuits. The utilization of circuits varies with circuit yield and routing density, but has generally been 60 to 70 percent of all the operative circuits. Figure A-2b shows a complete set of relocations for the four master pattern gates, assuming only the gates whose pads are not crossed out have passed all probe tests. The yield condition shown points out that even though the local yield is not 50 percent (i.e., 37 percent, since only three of eight circuits are operational), only rare yield distributions will prohibit relocation of circuits from adjacent areas. Experience with hundreds of wafers has confirmed this conclusion.

Following probe-cell test, after second level metallization, the required relocations are chosen by computer from the available set to accommodate the cell yield pattern. Since this relocation selection is accomplished at negligible cost, pad relocated LSI achieves low recurring costs at very high monolithic complexity. Moreover, since the system, by design, accounts forthe less than perfect circuit yield per wafer, it permits a low cost LSI implementation of any large logic circuit. Its cost advantages are particularly apparent for low volume military applications.

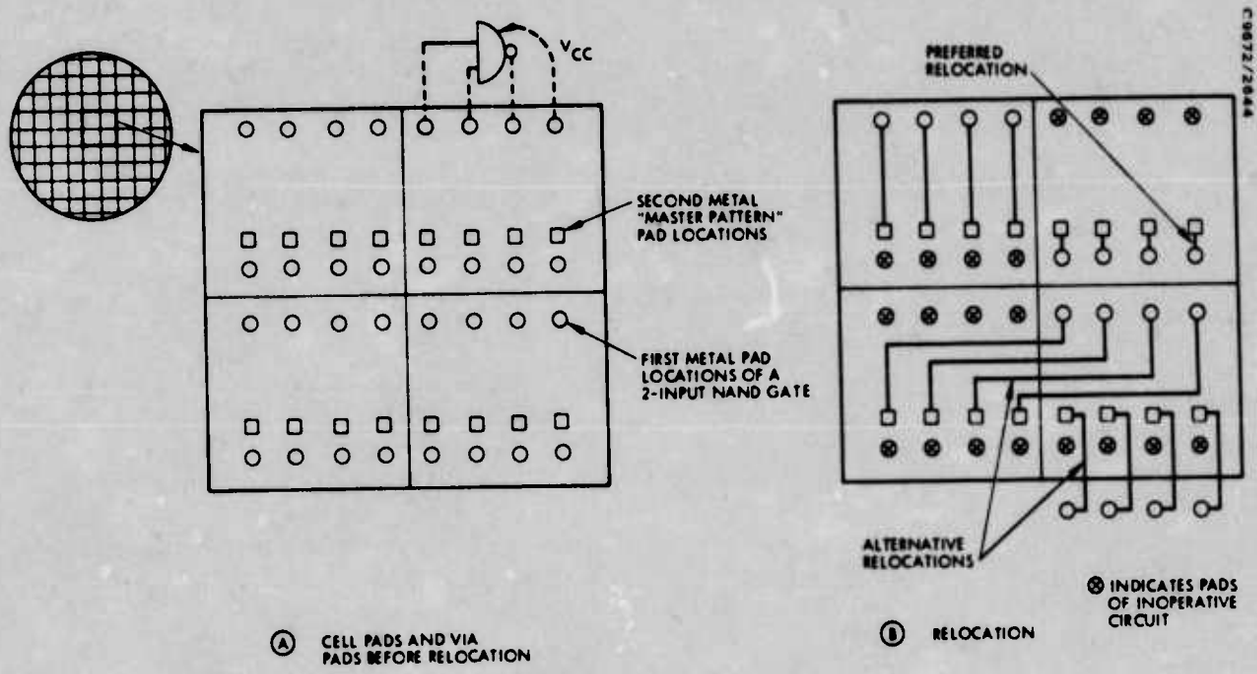


Figure A-2. Pad relocation technique.

In summary, in pad relocation, a master pattern and master pattern routing is generated only once for each logic part type. Standard relocation patterns have been generated for each cell type.

Hughes "Pad Relocation" capabilities include a standard cell library of SSI/MSI TTL circuit types, along with the required wafer and multilevel metallization processing technology. These provide a complete state-of-the-art LSI design and fabrication capability most suited to demonstrate advantages of custom LSI for low volume military production.

At Hughes, full (and partial) wafers (of SSI, MSI, and/or custom cells) have been developed to achieve LSI through the batch processed interconnection of a large number of standard circuits on a monolithic array. The pad relocation approach emphasizes high density circuit interconnections while also achieving a higher level of packaging.

Full or partial wafer arrays and custom high density LSI are also packaged together. Systems incorporating both full wafer LSI and hybrid packages containing 100 percent yield custom LSI chip and partial wafer LSI are being used to permit extremely high levels of system circuit integrations.

*U.S.Government Printing Office: 1974 — 657-014/159